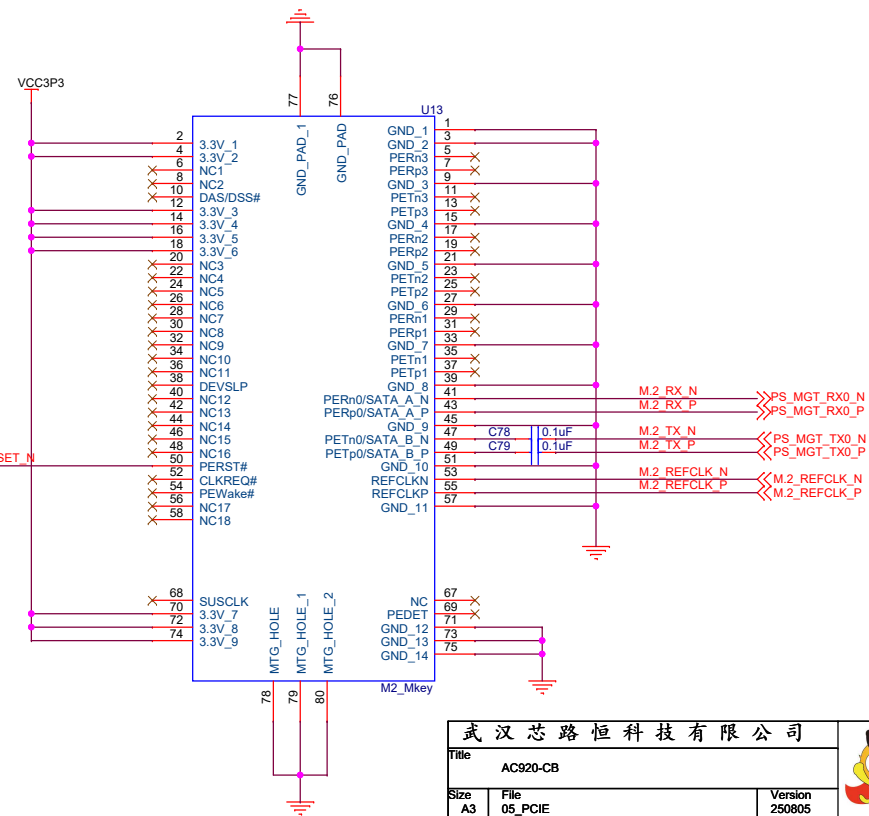
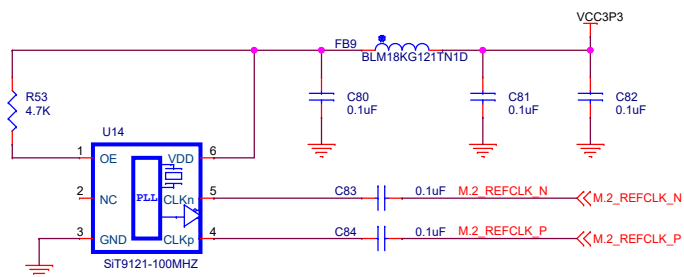
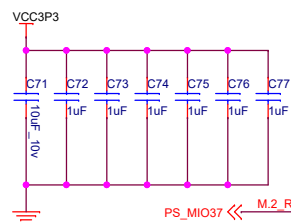
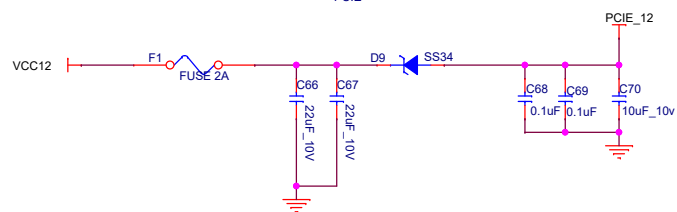
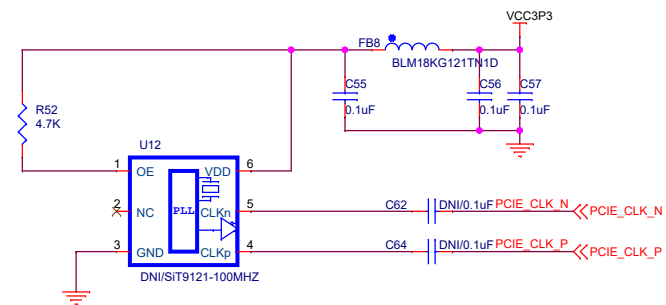
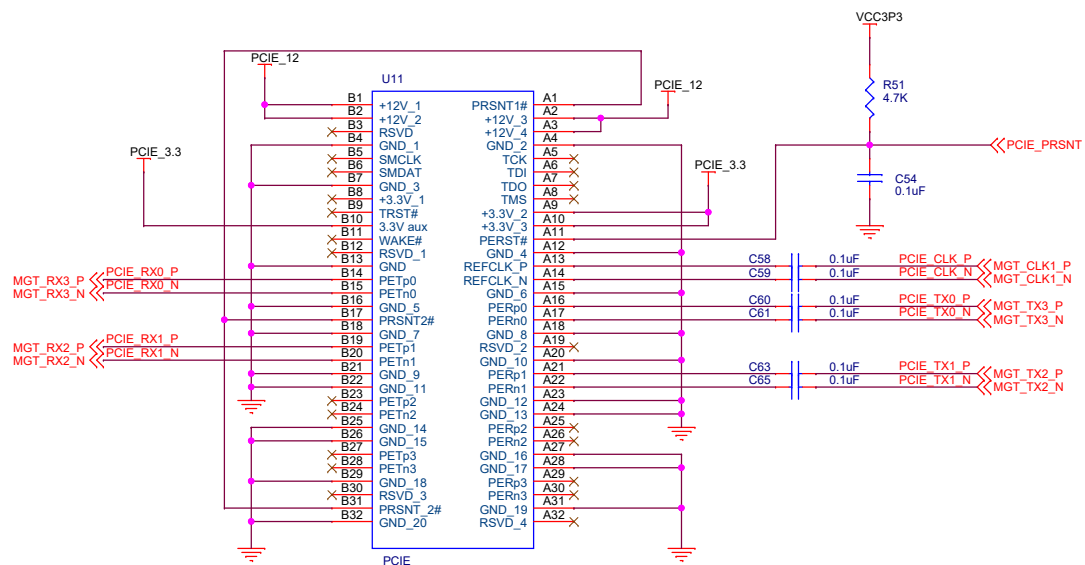


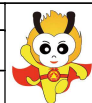


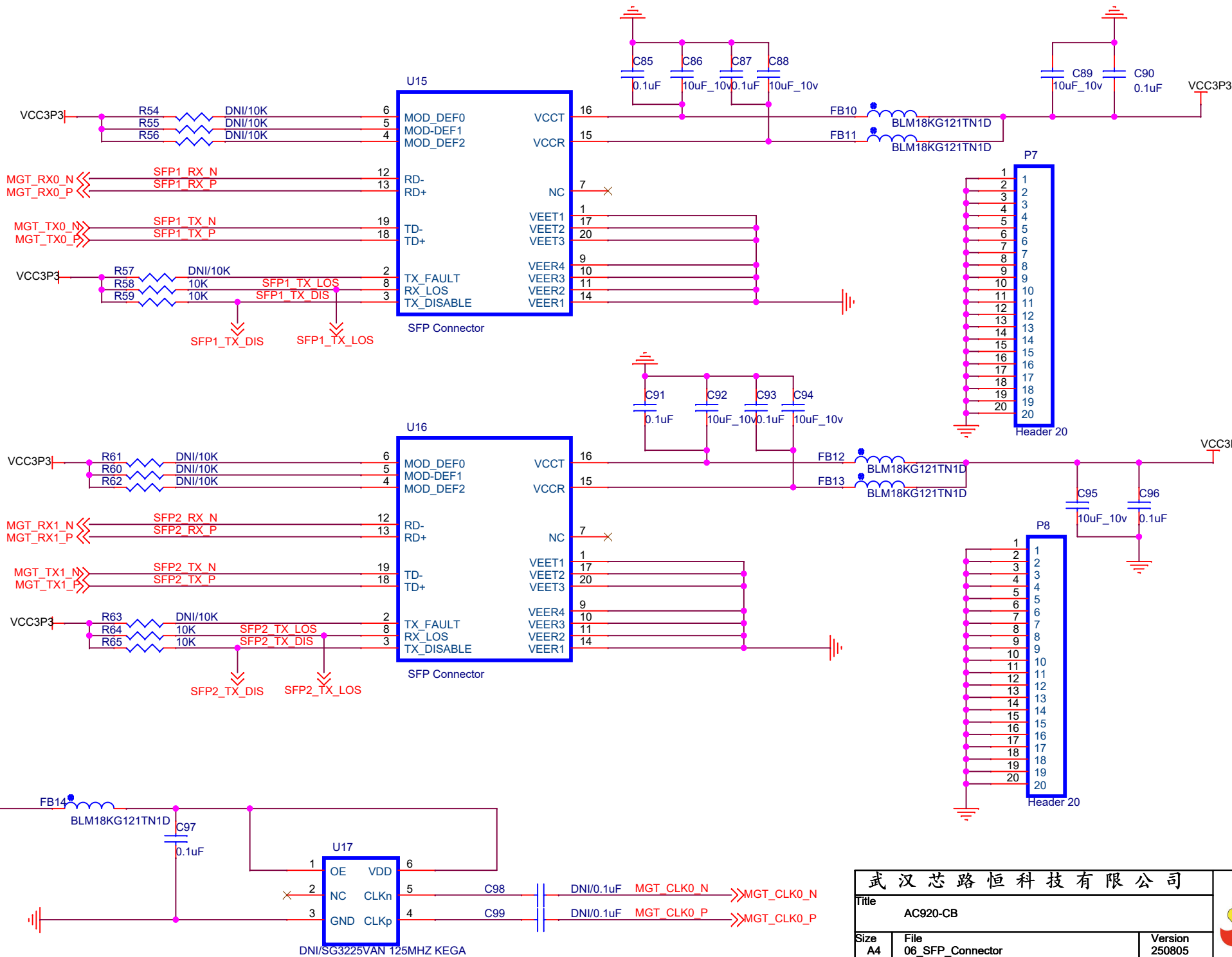
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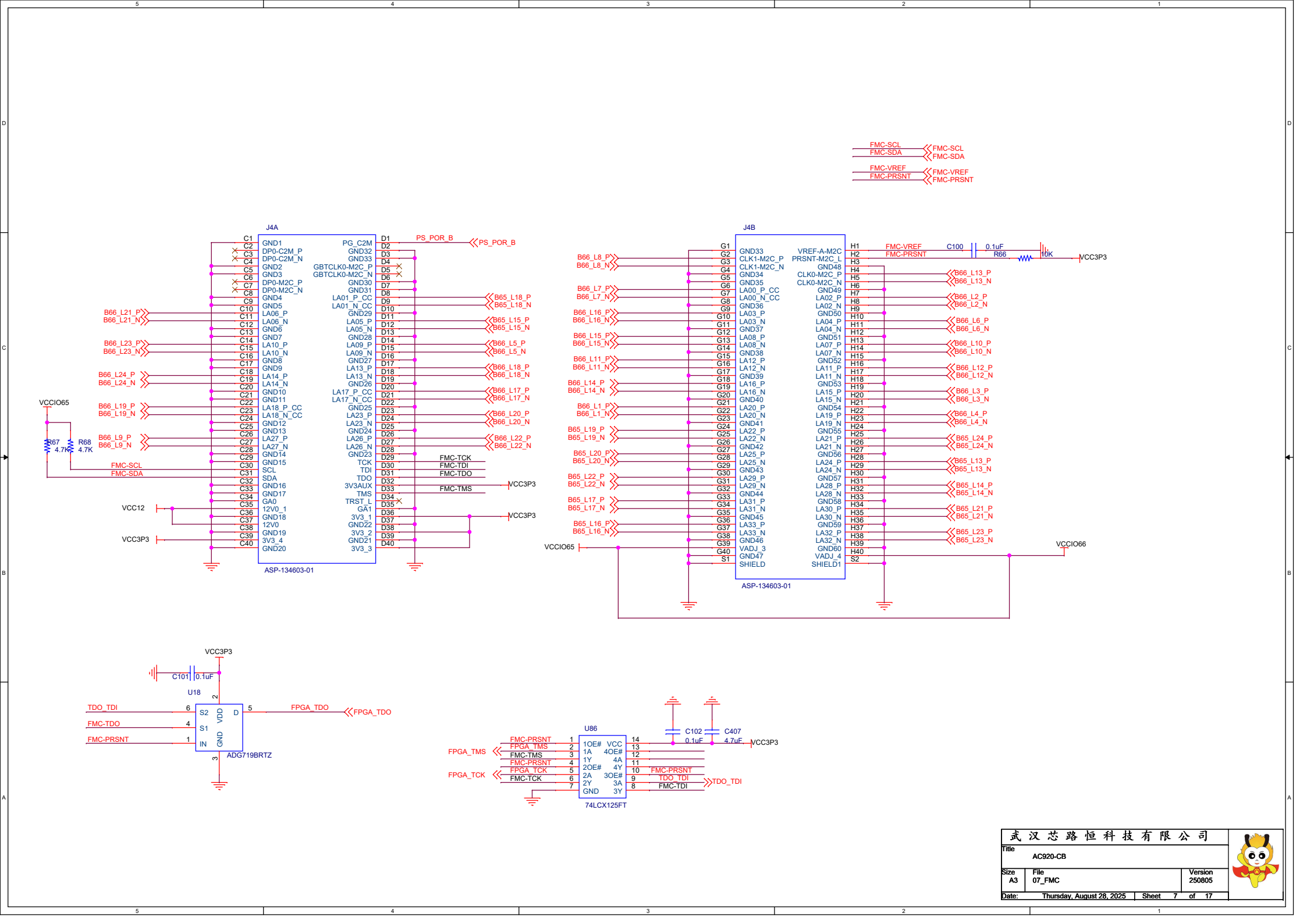
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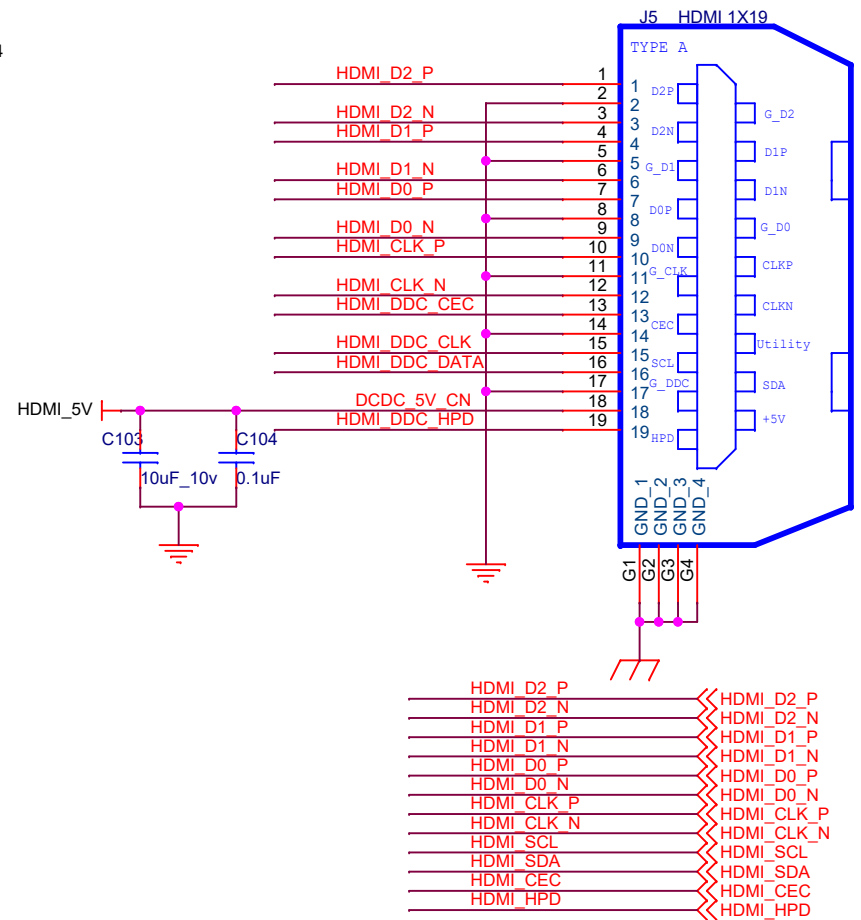
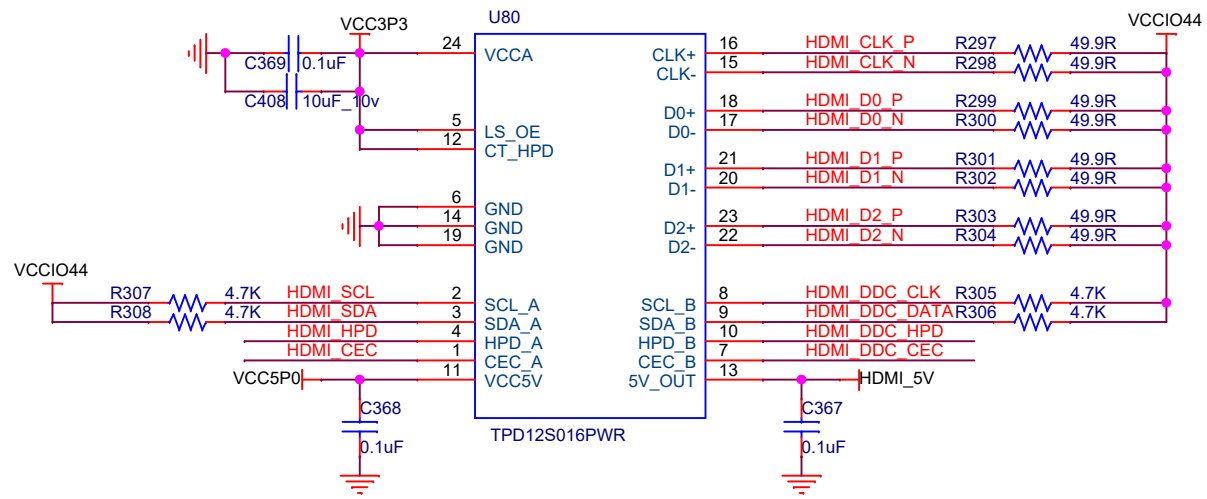
Size A3 File 05_PCIE Version 250805

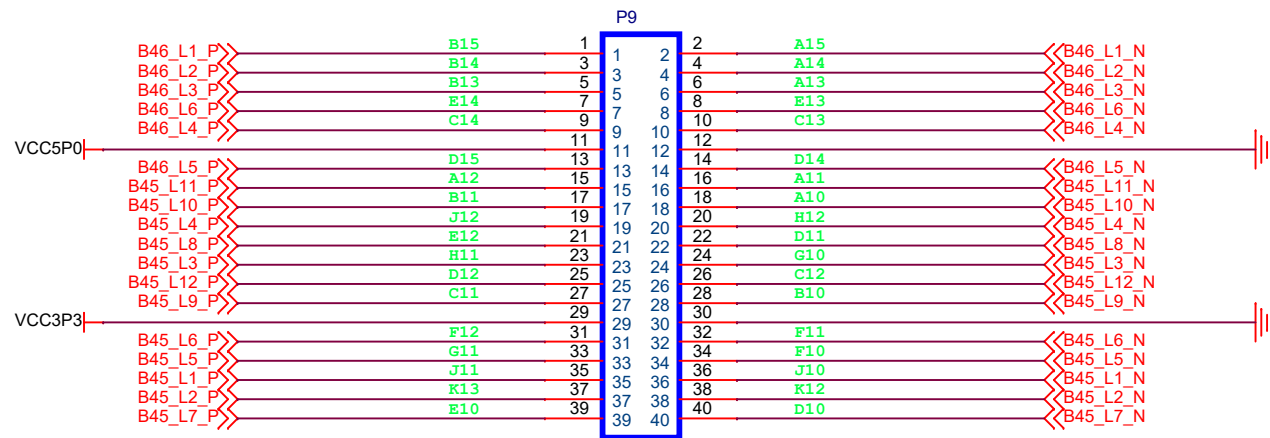
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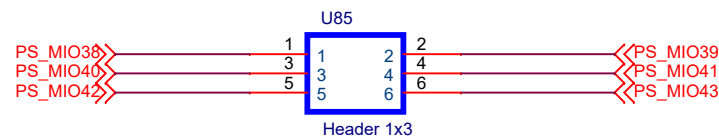




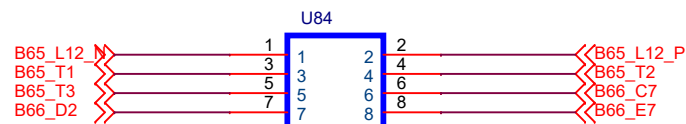
Header 20X2

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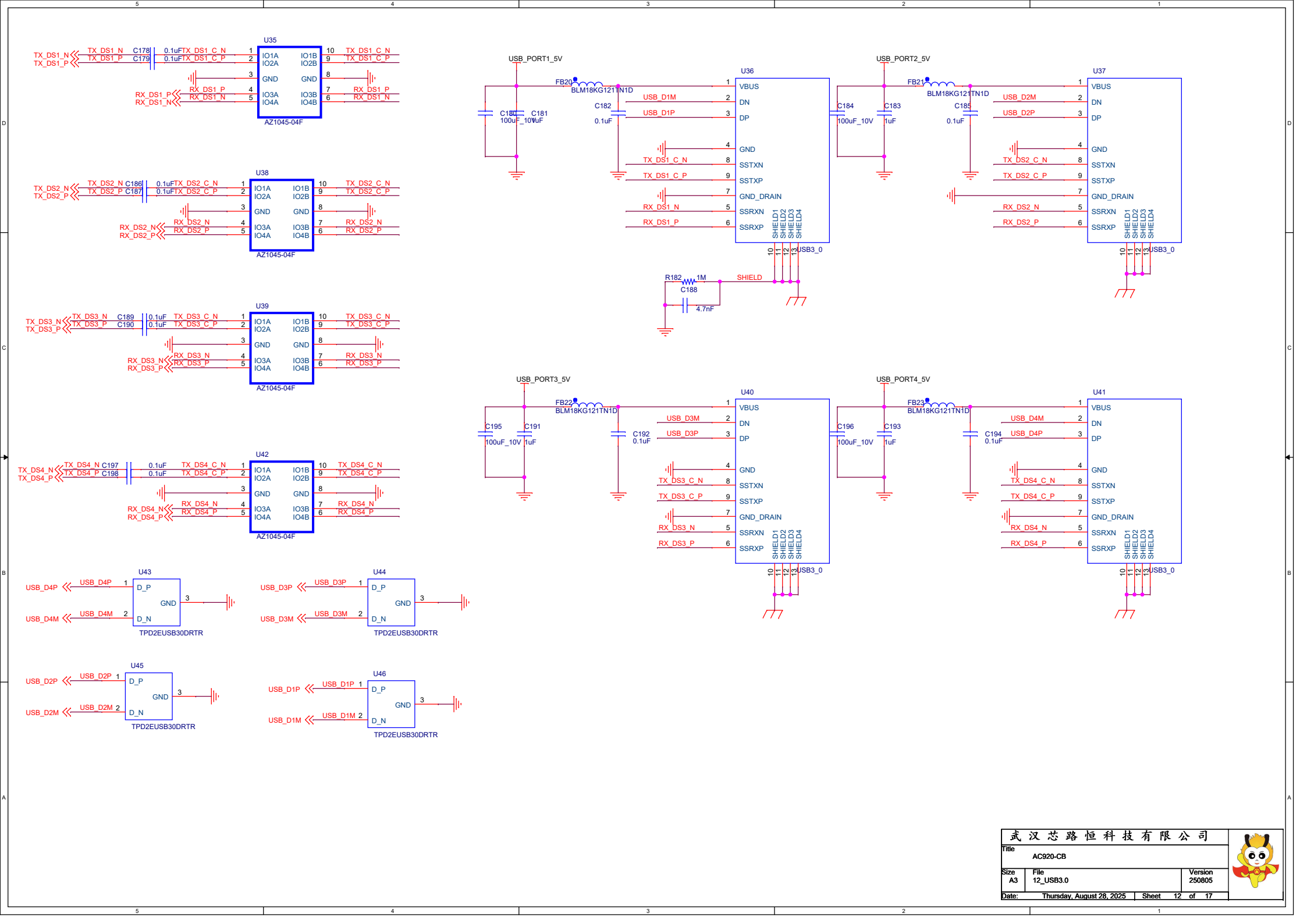
兼容DE2的通用扩展接口

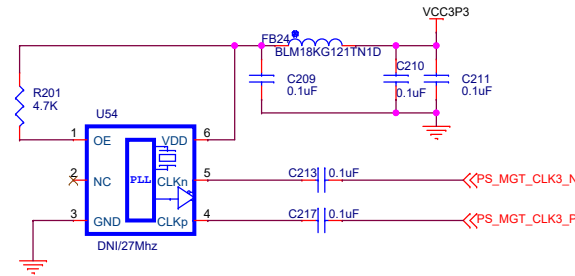
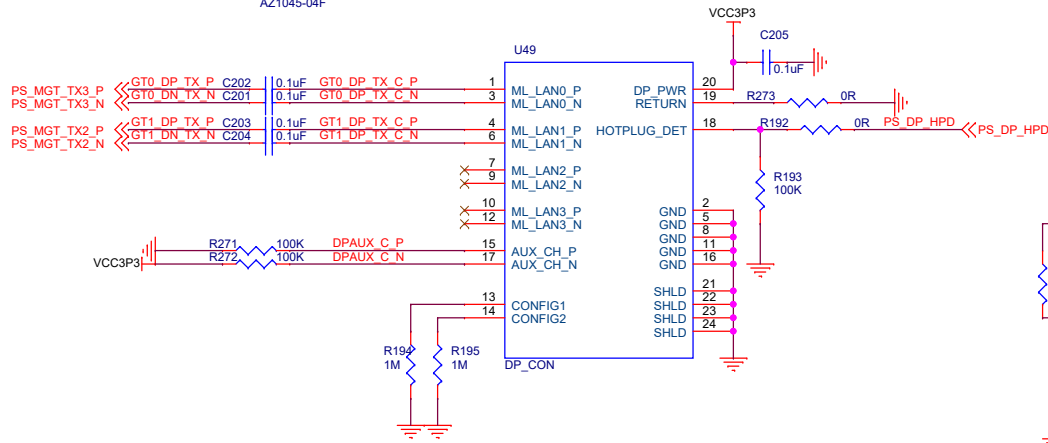
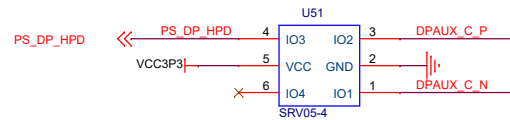
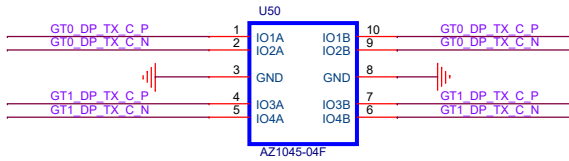
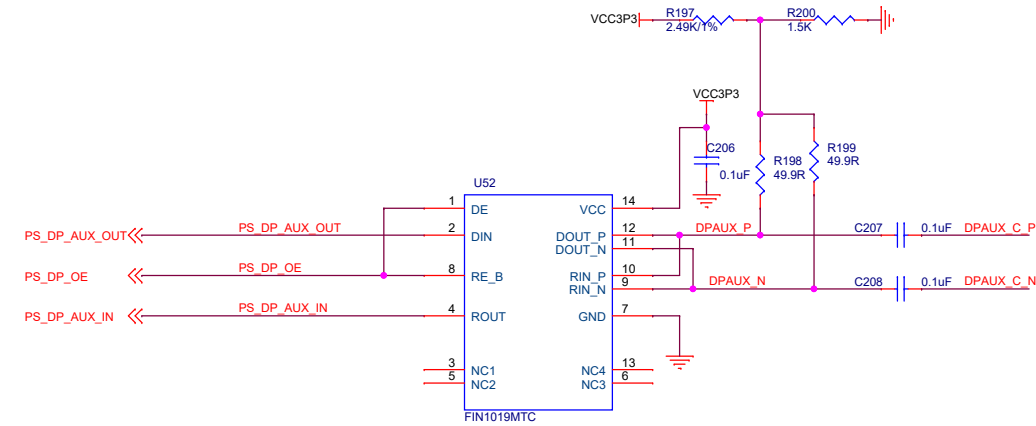


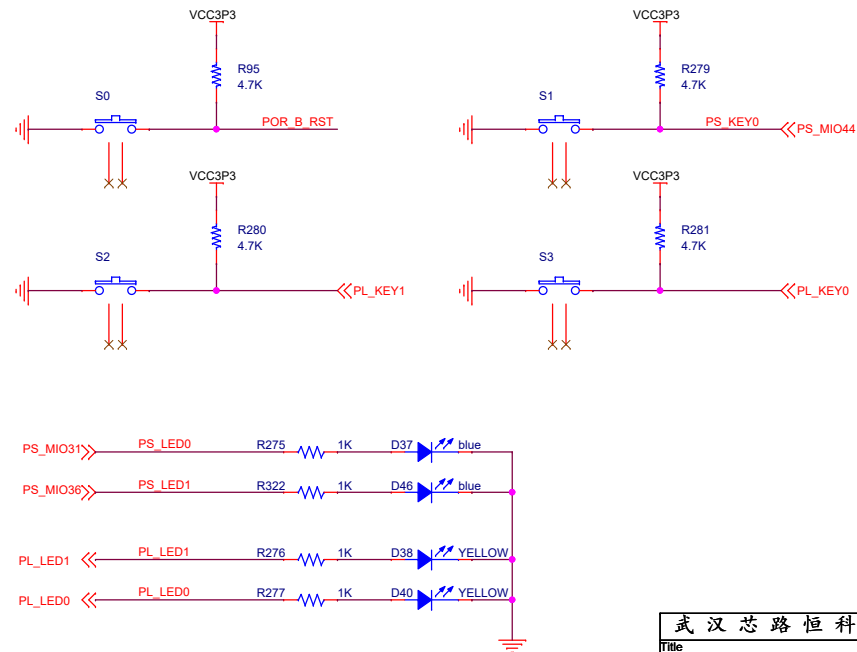
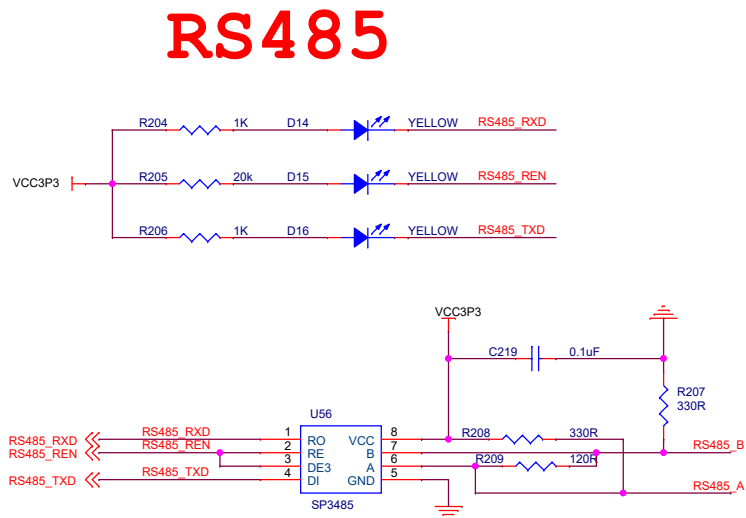
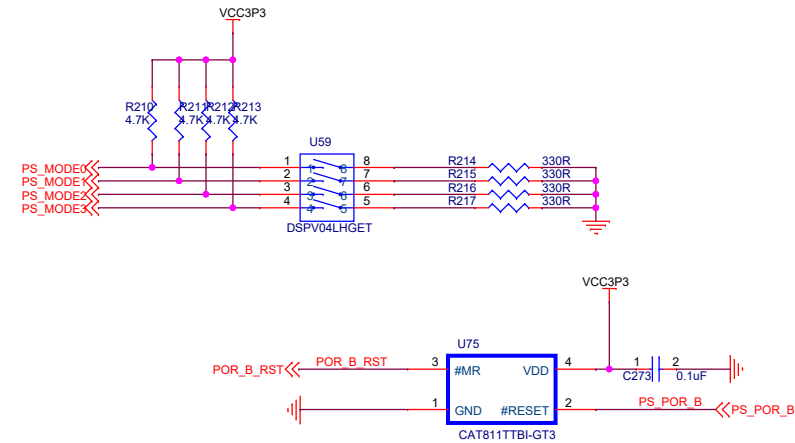
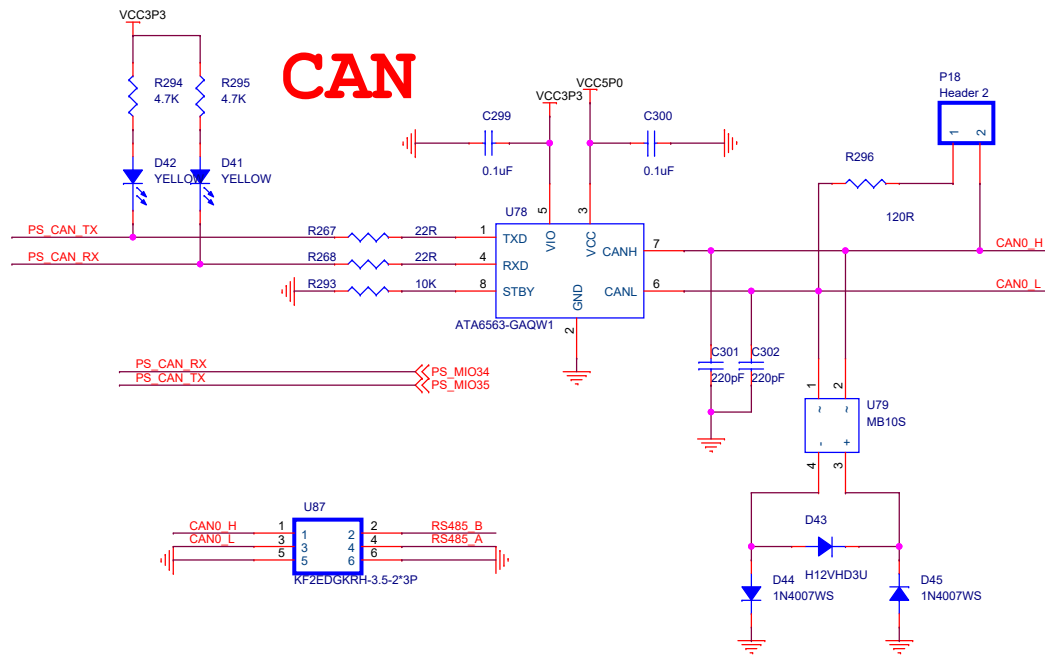
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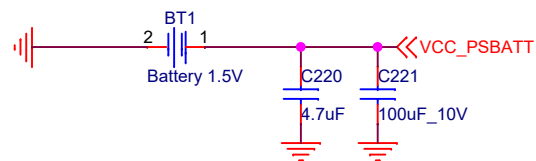
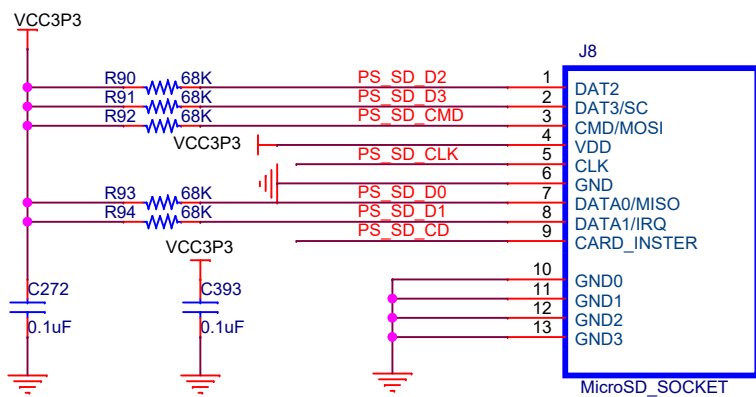
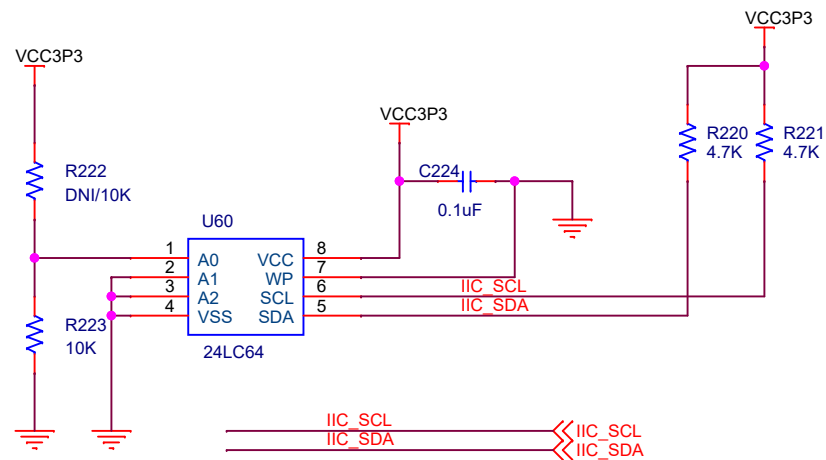
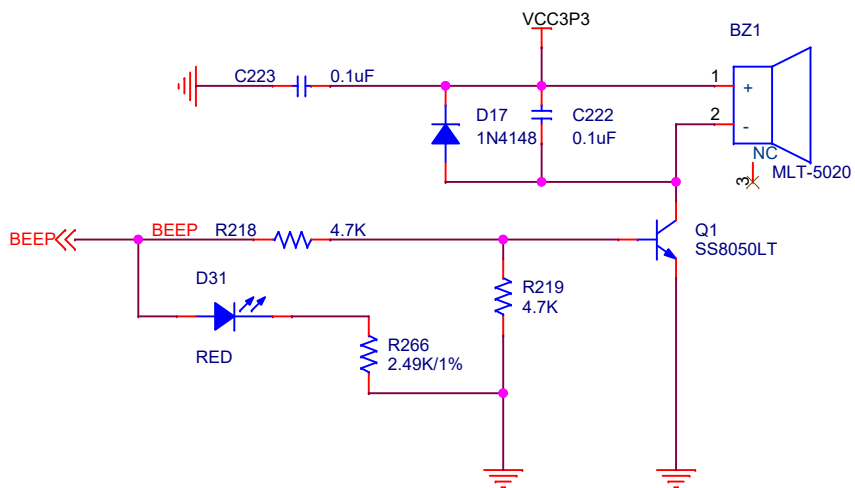


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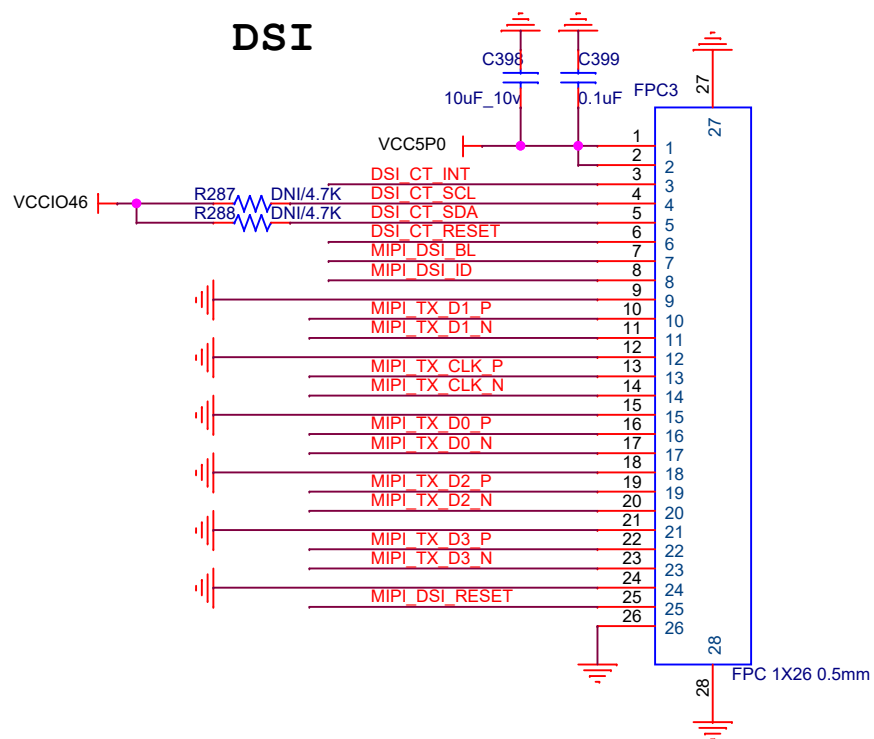








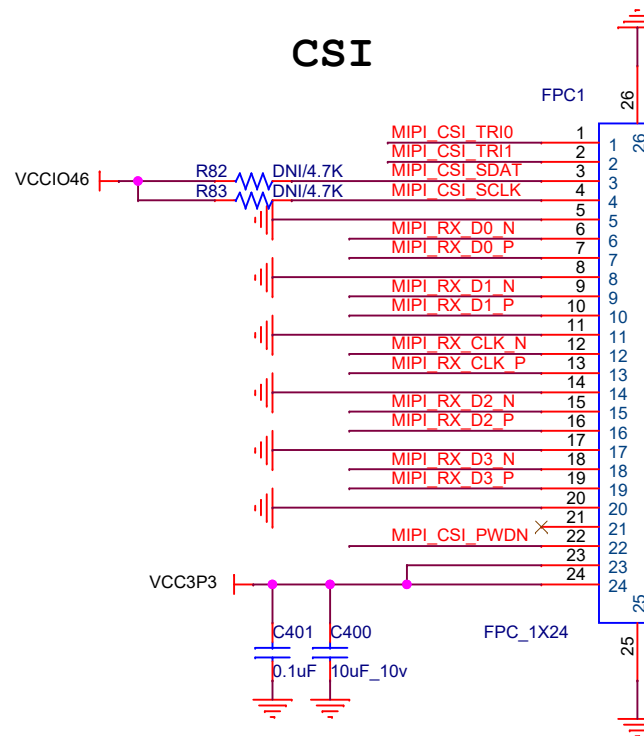
DSI



DSI CT INT << DSI_CT_INT
 DSI CT SCL << DSI_CT_SCL
 DSI CT SDA << DSI_CT_SDA
 DSI CT RESET << DSI_CT_RESET
 MIPI DSI BL << MIPI_DSI_BL
 MIPI DSI ID << MIPI_DSI_ID
 MIPI DSI RESET << MIPI_DSI_RESET

MIPI TX D0 N << B65_L7_N
 MIPI TX D0 P << B65_L7_P
 MIPI TX D1 N << B65_L8_N
 MIPI TX D1 P << B65_L8_P
 MIPI TX CLK N << B65_L11_N
 MIPI TX CLK P << B65_L11_P
 MIPI TX D2 N << B65_L9_N
 MIPI TX D2 P << B65_L9_P
 MIPI TX D3 N << B65_L10_N
 MIPI TX D3 P << B65_L10_P

CSI



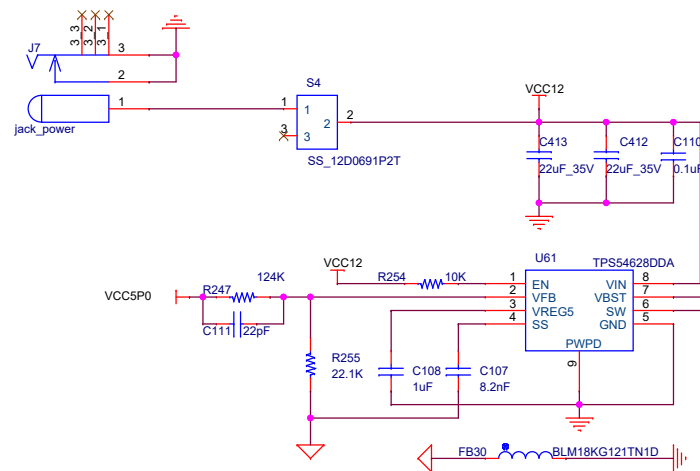
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 MIPI CSI SDAT << MIPI_CSI_SDAT
 MIPI CSI SCLK << MIPI_CSI_SCLK
 MIPI CSI PWDN << MIPI_CSI_PWDN

MIPI RX D0 P << B65_L2_P
 MIPI RX D0 N << B65_L2_N
 MIPI RX D1 P << B65_L3_P
 MIPI RX D1 N << B65_L3_N
 MIPI RX D2 P << B65_L4_P
 MIPI RX D2 N << B65_L4_N
 MIPI RX D3 P << B65_L5_P
 MIPI RX D3 N << B65_L5_N
 MIPI RX CLK P << B65_L1_P
 MIPI RX CLK N << B65_L1_N

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$$V_{out} = 0.765 \times (1 + R1/R2)$$

