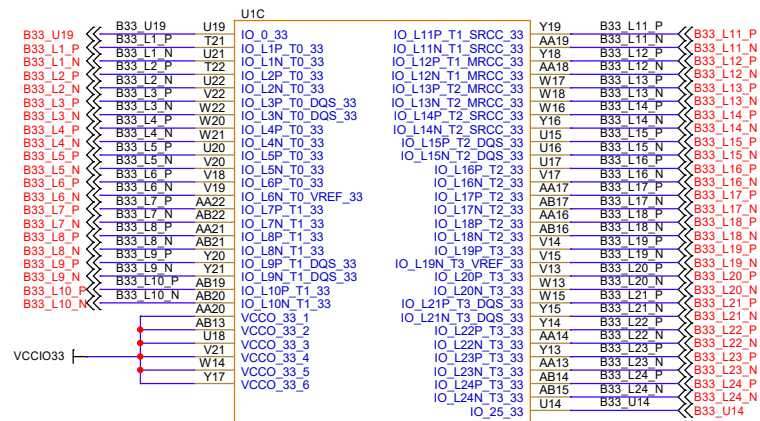
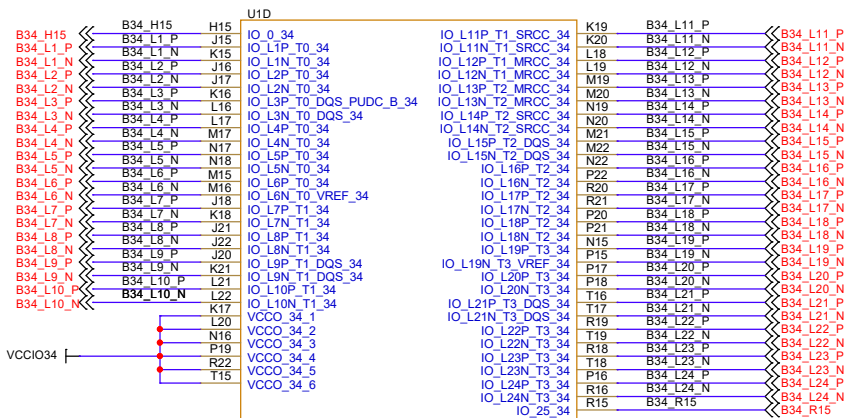


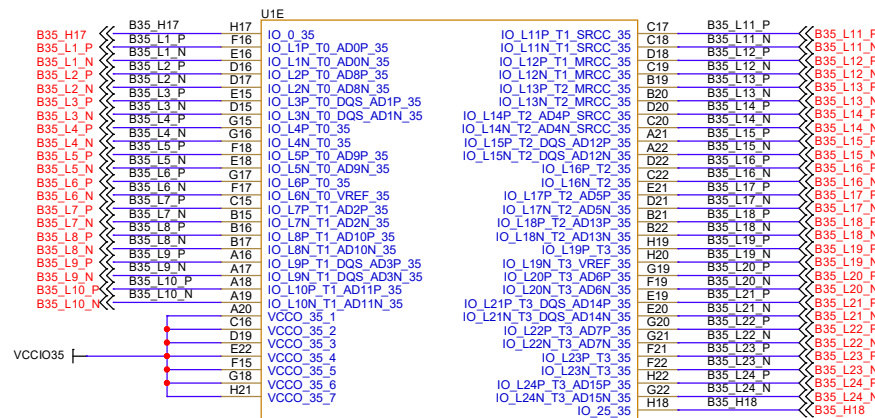
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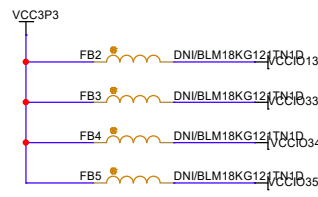
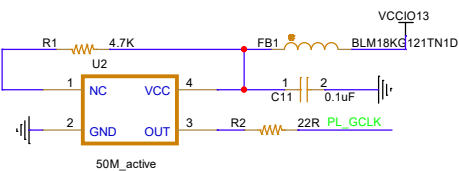
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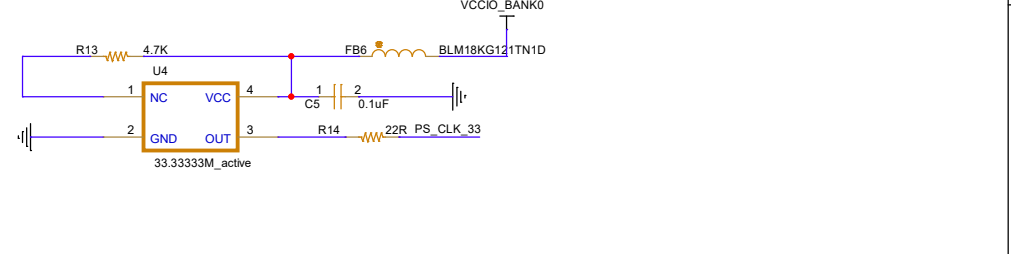
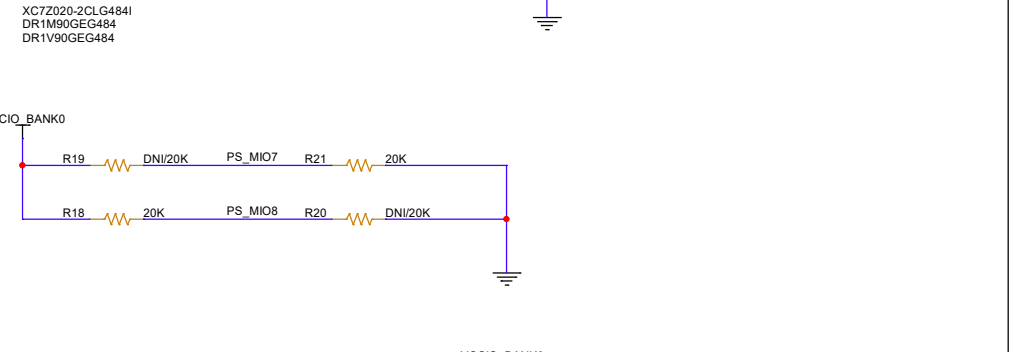
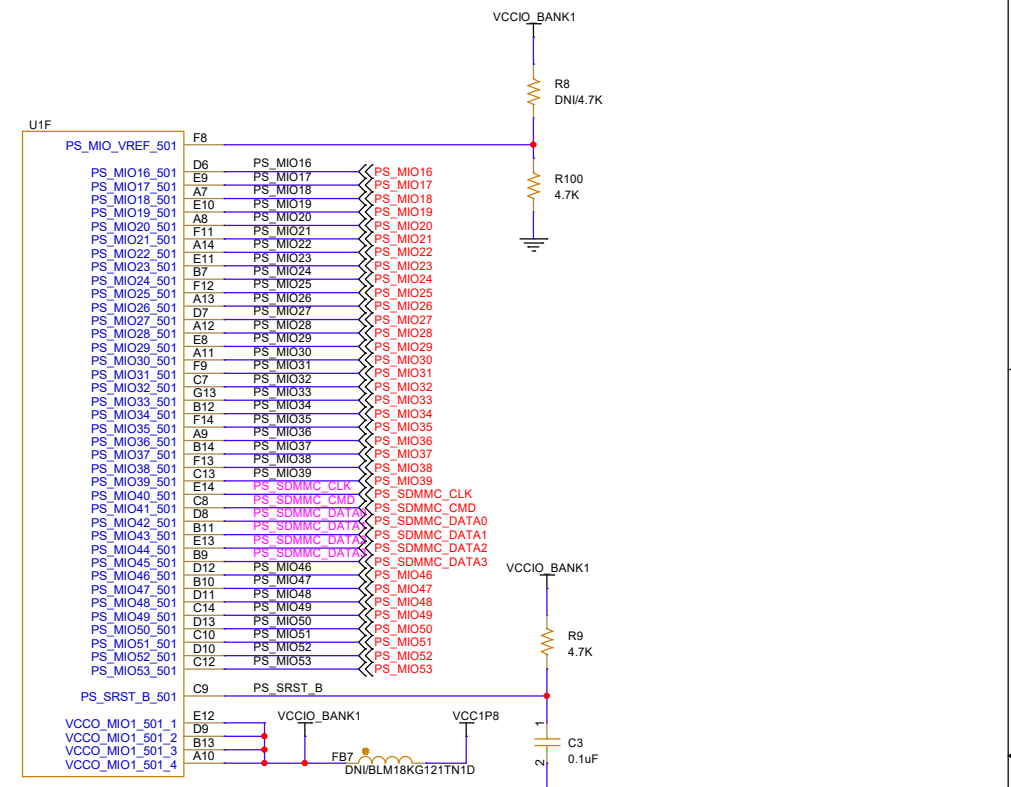
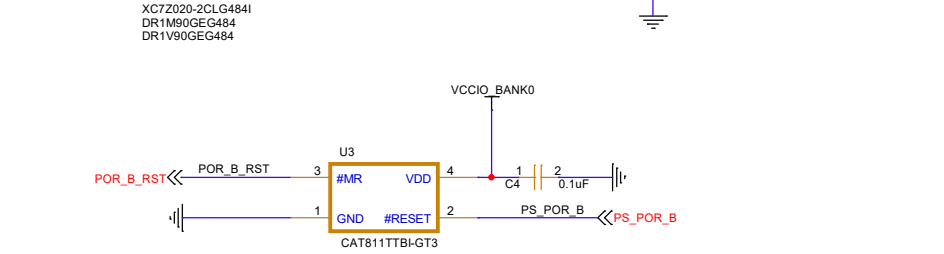
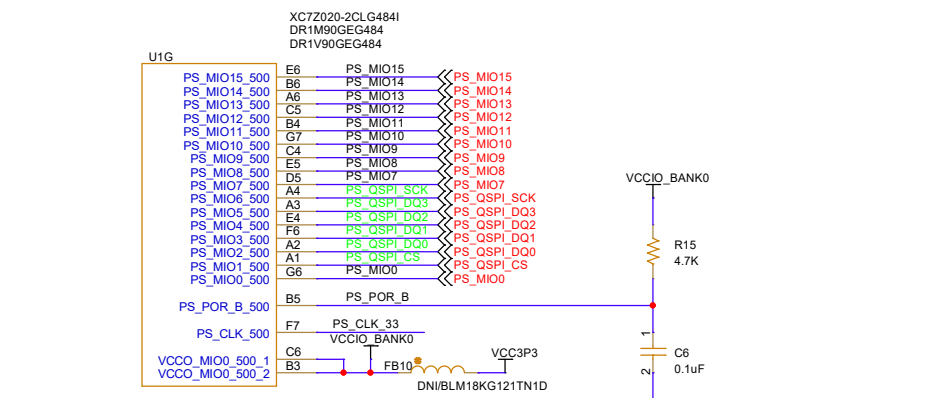
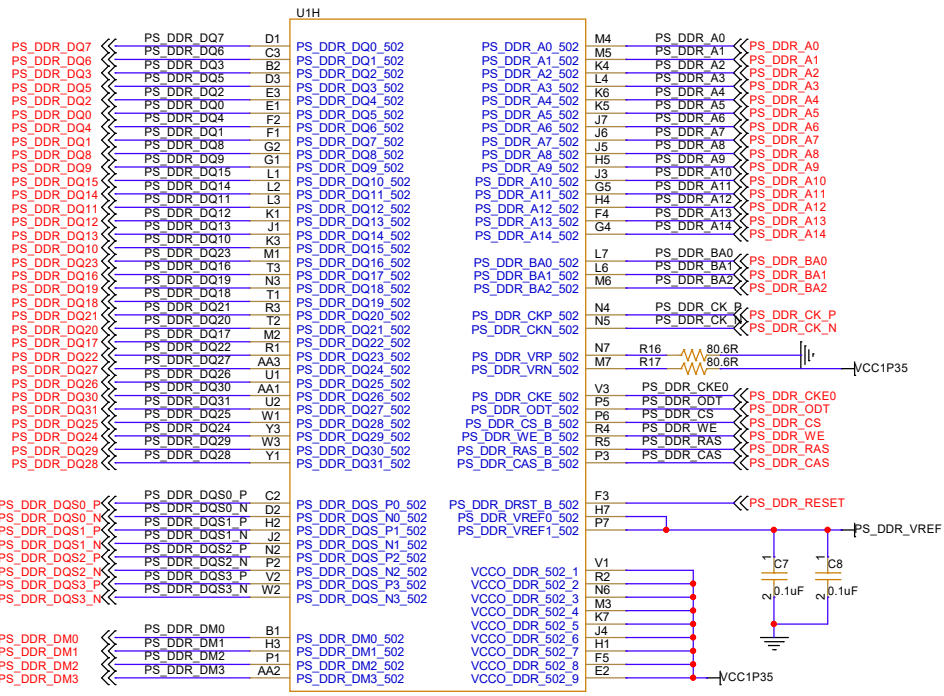


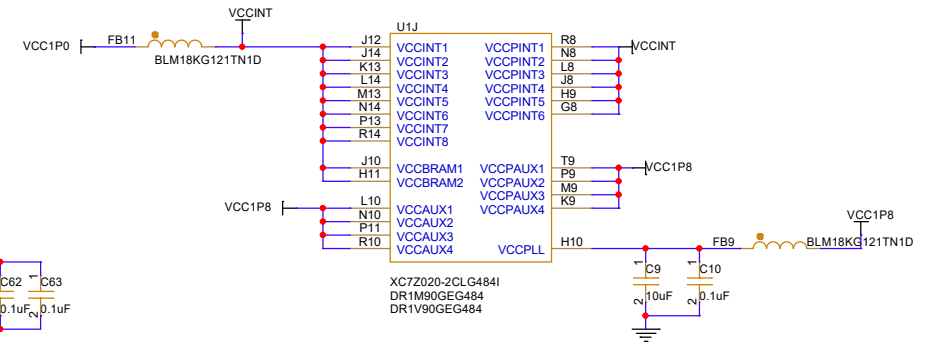
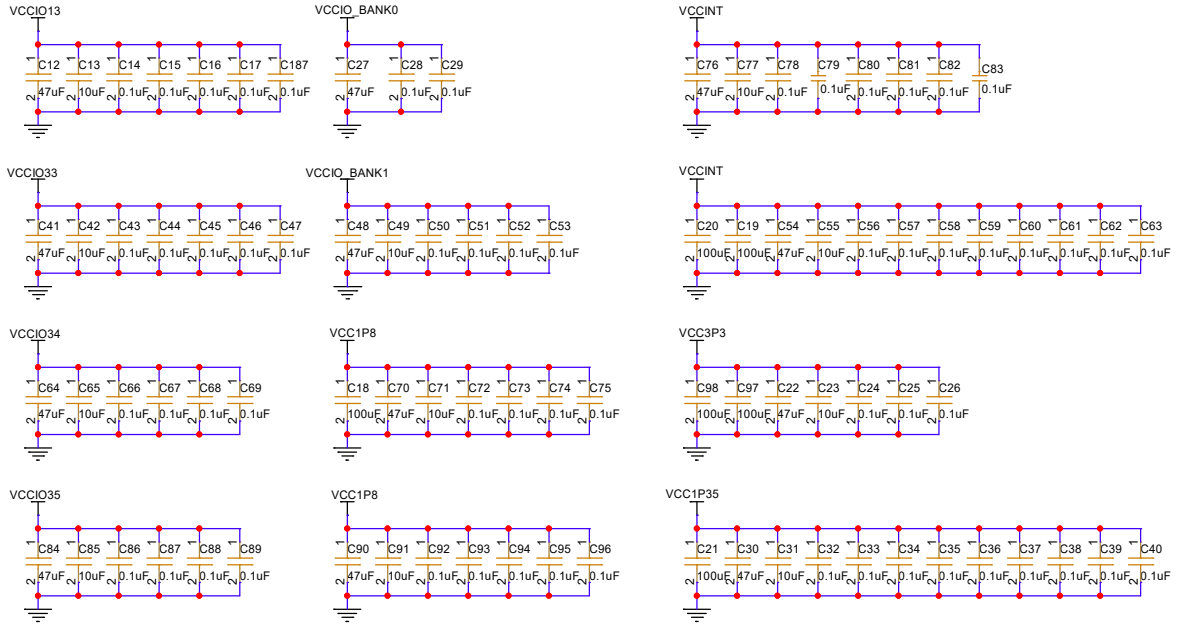
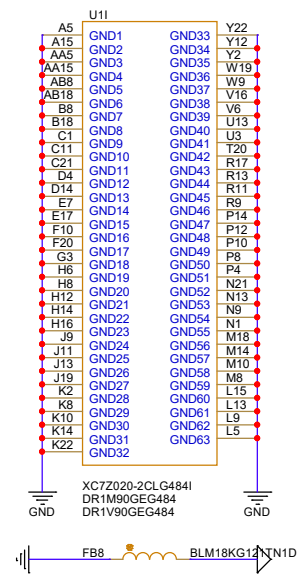
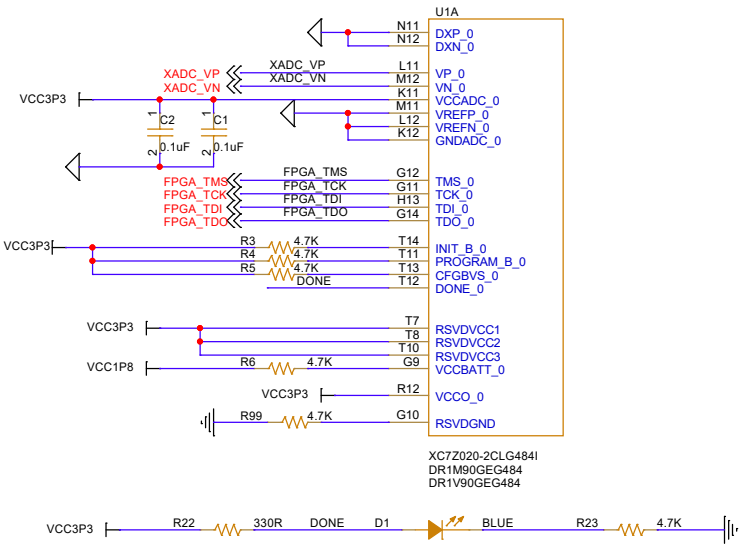
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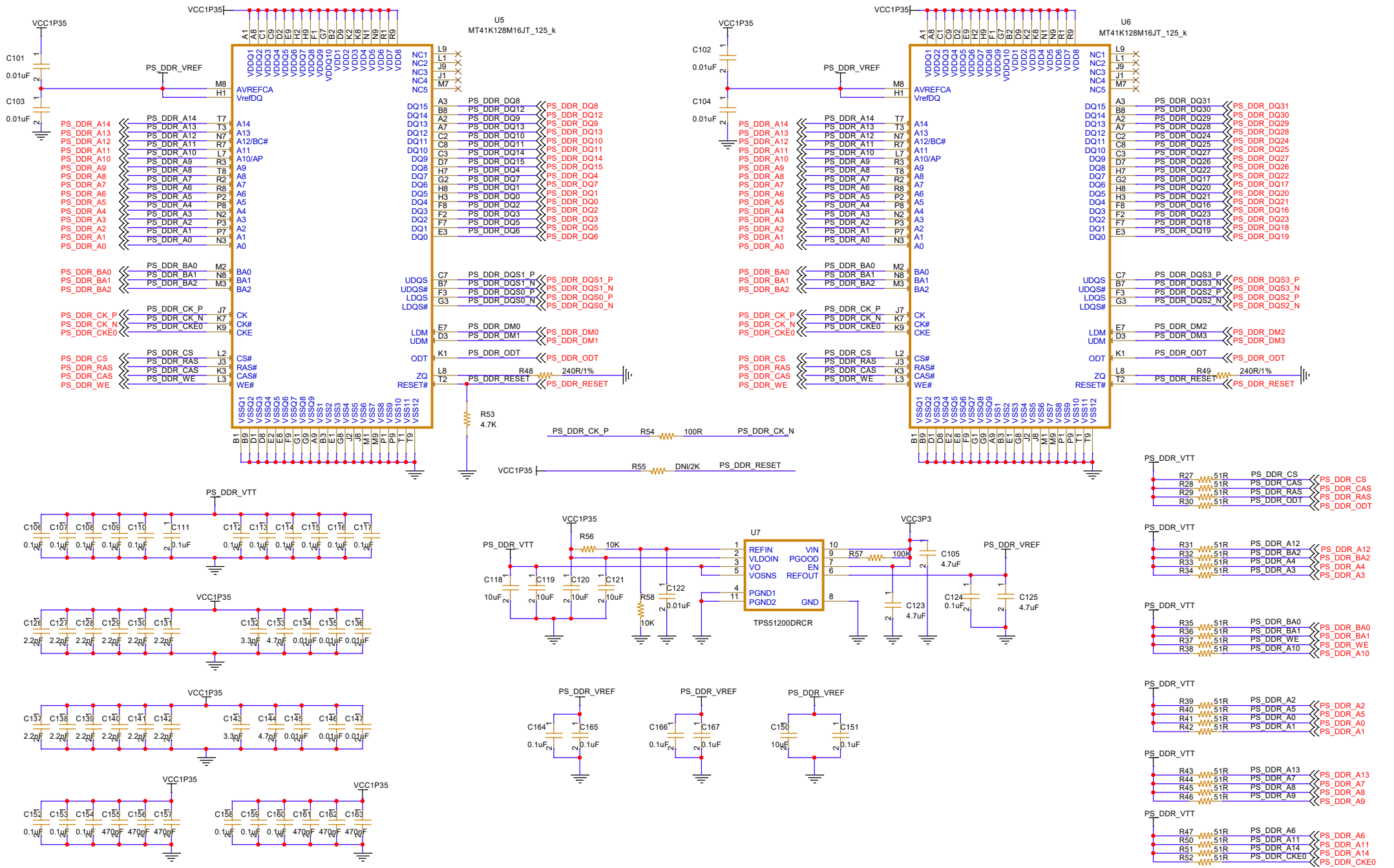


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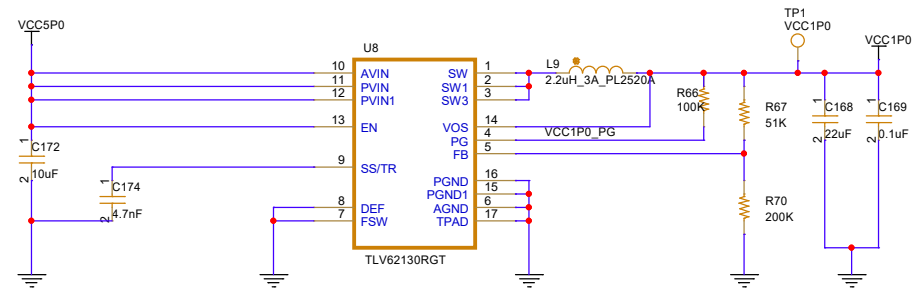




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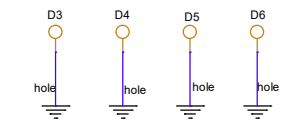
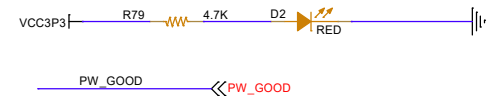
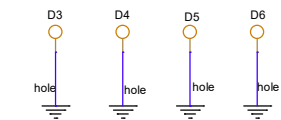
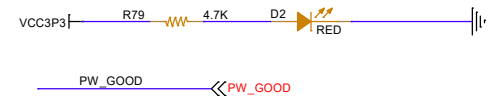
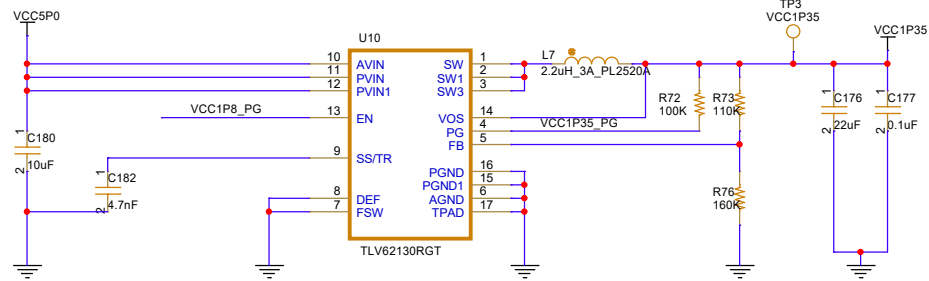
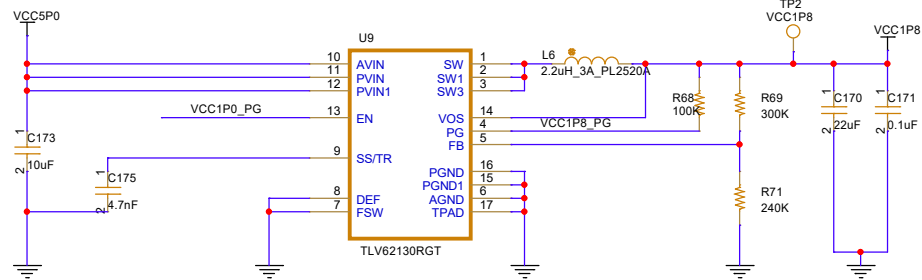
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$R1=R2 (v_{out}/0.8-1)$
 R1 R2 VOUT
 51K 200K 1.0
 51K 270K 0.95

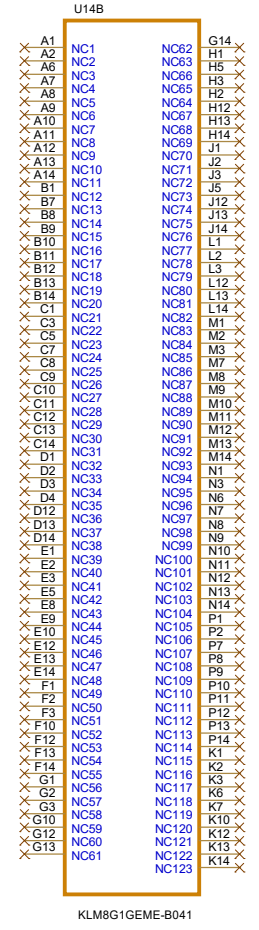
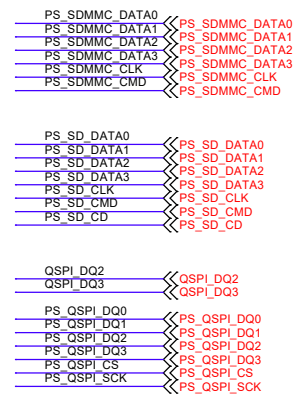
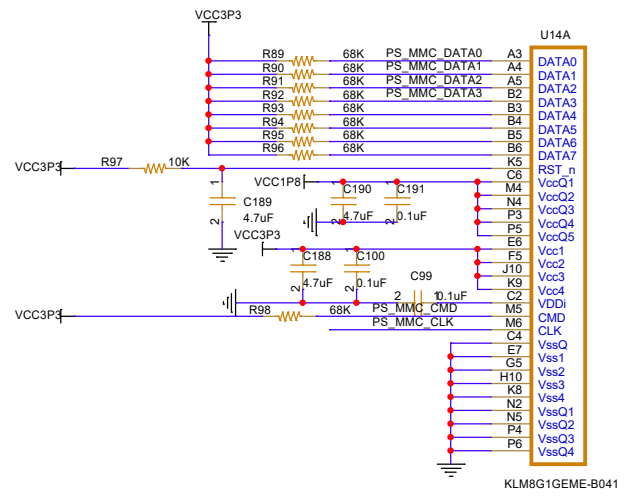
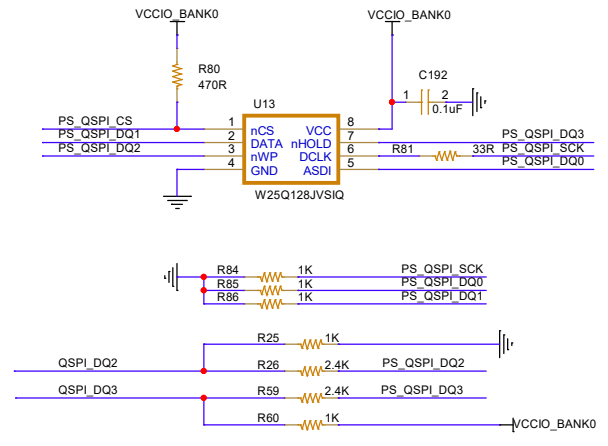
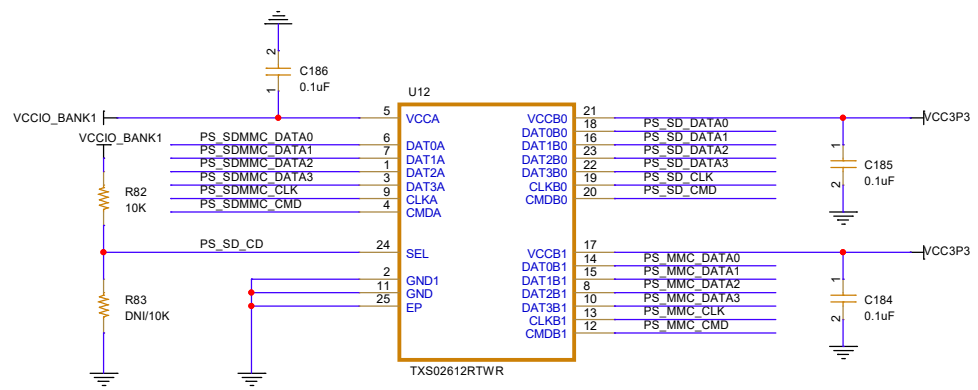
Xilinx版本
 安路版本



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