

A

B

C

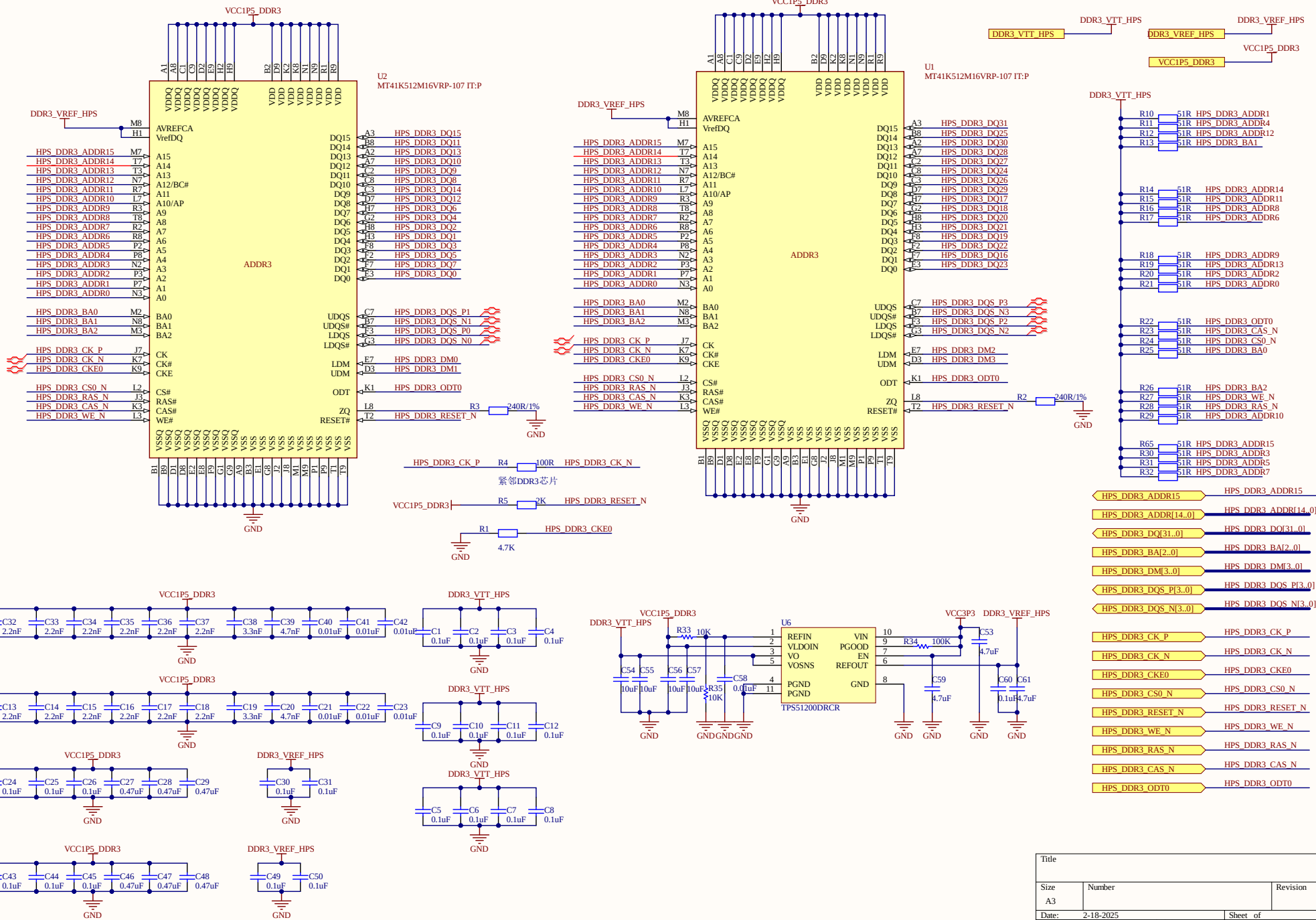
D

A

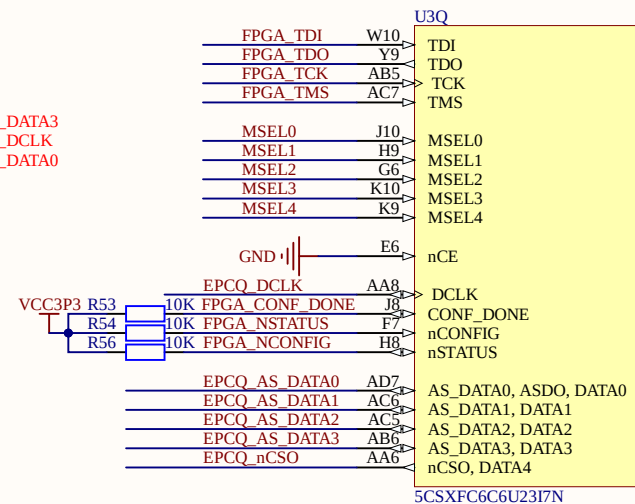
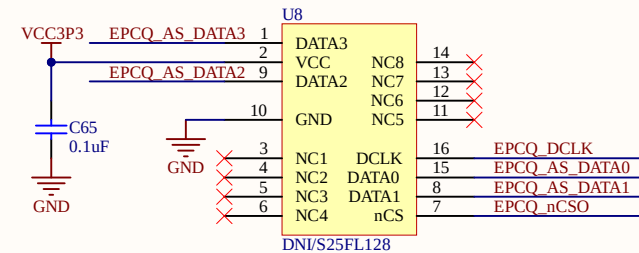
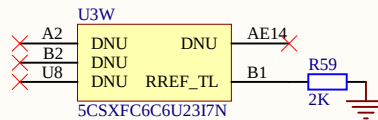
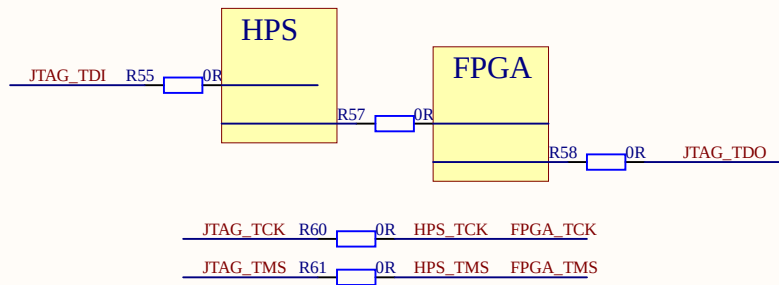
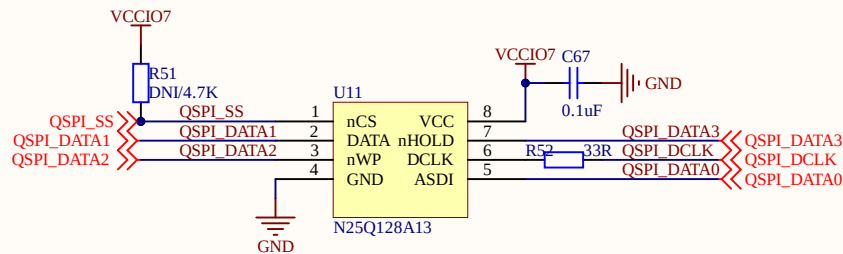
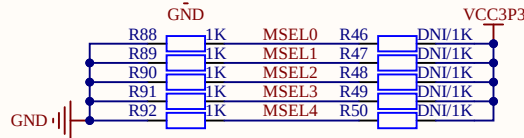
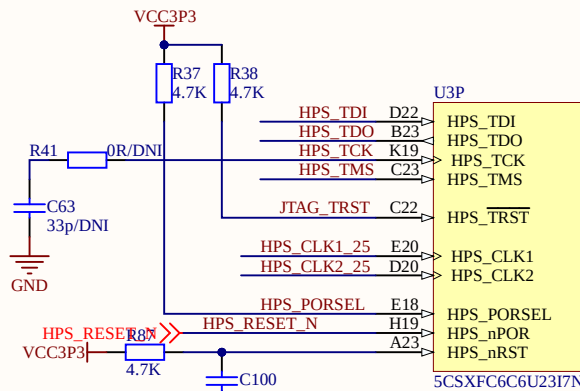
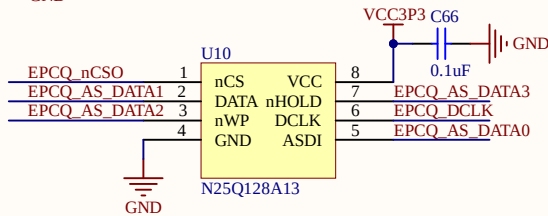
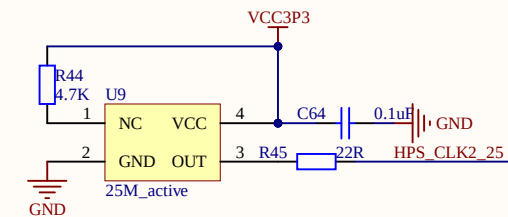
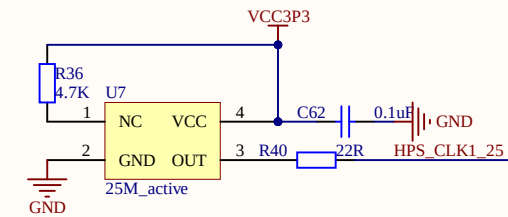
B

C

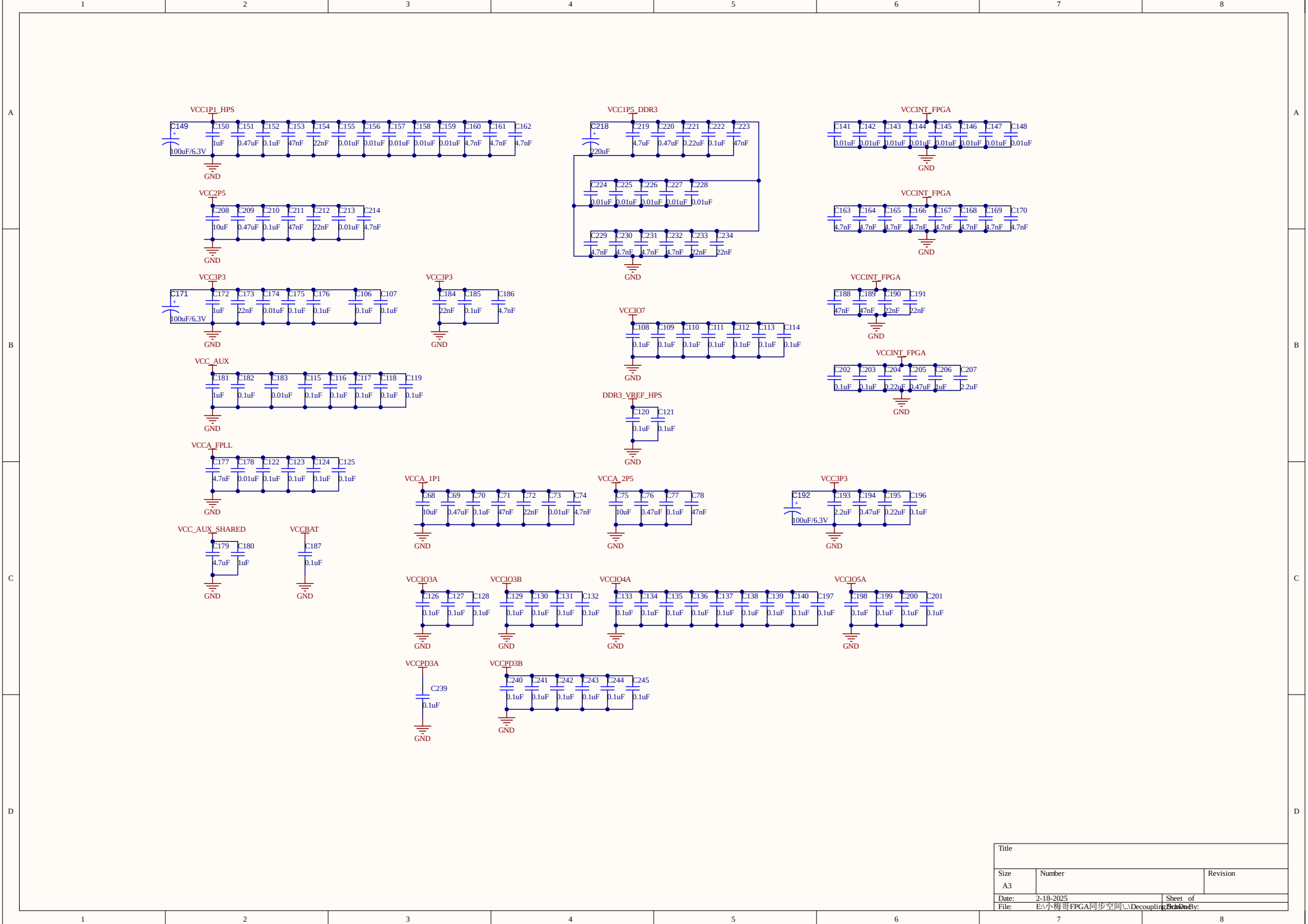
D



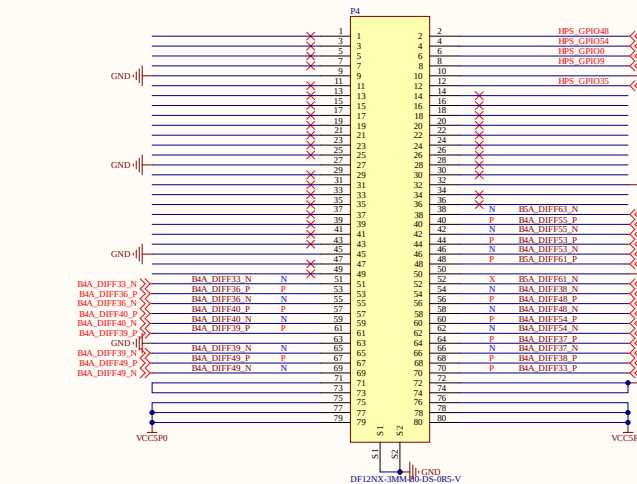
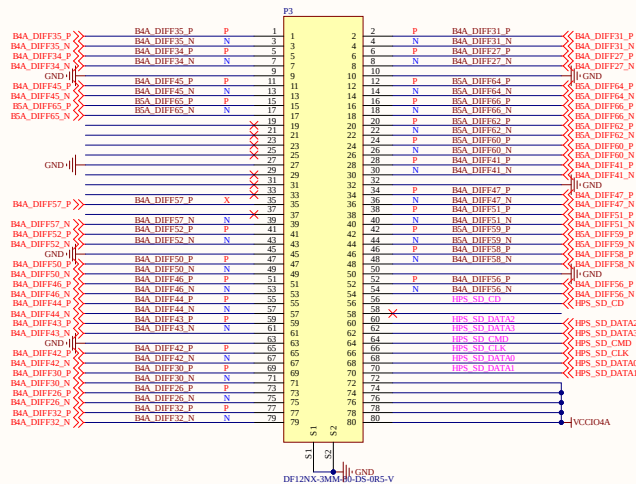
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File:	E:\小梅哥FPGA同步空间\DDR3.Sch	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2-18-2025	Sheet of
File:	E:\小梅哥\FPGA同步空间\HPS_CFG_Schematic	Drawn By:



Title		
Size A3	Number	Revision
Date: 2-18-2025		Sheet of
File: E:\小梅哥FPGA同步空间\Decoupling		By: 小梅哥



U3F

BANK 6A

HPS_DDR, (, , , , HPS_A_0, HPS_CA_0)
HPS_DDR, (, , , , HPS_A_1, HPS_CA_1)
HPS_DDR, (, , , , HPS_A_2, HPS_CA_2)
HPS_DDR, (, , , , HPS_A_3, HPS_CA_3)
HPS_DDR, (, , , , HPS_A_4, HPS_CA_4)
HPS_DDR, (, , , , HPS_A_5, HPS_CA_5)
HPS_DDR, (, , , , HPS_A_6, HPS_CA_6)
HPS_DDR, (, , , , HPS_A_7, HPS_CA_7)
HPS_DDR, (, , , , HPS_A_8, HPS_CA_8)
HPS_DDR, (, , , , HPS_A_9, HPS_CA_9)
HPS_DDR, (, , , , HPS_A_10, HPS_CA_10)
HPS_DDR, (, , , , HPS_A_11, HPS_CA_11)
HPS_DDR, (, , , , HPS_A_12, HPS_CA_12)
HPS_DDR, (, , , , HPS_A_13, HPS_CA_13)
HPS_DDR, (, , , , HPS_A_14, HPS_CA_14)
HPS_DDR, (, , , , HPS_A_15, HPS_CA_15)

HPS_DDR, (, , , , HPS_BA_0)
HPS_DDR, (, , , , HPS_BA_1)
HPS_DDR, (, , , , HPS_BA_2)

HPS_DDR, (, , , , HPS_CK, HPS_CK)
HPS_DDR, (, , , , HPS_CK#, HPS_CK#)
HPS_DDR, (, , , , HPS_CKE_0, HPS_CKE_0)
HPS_DDR, (, , , , HPS_CKE_1, HPS_CKE_1)

HPS_DDR, (, , , , HPS_WE#)
HPS_DDR, (, , , , HPS_CAS#)
HPS_DDR, (, , , , HPS_RAS#)
HPS_DDR, (, , , , HPS_CS#_0, HPS_CS#_0)
HPS_DDR, (, , , , HPS_CS#_1, HPS_CS#_1)

HPS_DDR, (, , , , HPS_DQ_0, HPS_DQ_0)
HPS_DDR, (, , , , HPS_DQ_1, HPS_DQ_1)
HPS_DDR, (, , , , HPS_DQ_2, HPS_DQ_2)
HPS_DDR, (, , , , HPS_DQ_3, HPS_DQ_3)
HPS_DDR, (, , , , HPS_DQ_4, HPS_DQ_4)
HPS_DDR, (, , , , HPS_DQ_5, HPS_DQ_5)
HPS_DDR, (, , , , HPS_DQ_6, HPS_DQ_6)
HPS_DDR, (, , , , HPS_DQ_7, HPS_DQ_7)
HPS_DDR, (, , , , HPS_DQ_8, HPS_DQ_8)
HPS_DDR, (, , , , HPS_DQ_9, HPS_DQ_9)
HPS_DDR, (, , , , HPS_DQ_10, HPS_DQ_10)
HPS_DDR, (, , , , HPS_DQ_11, HPS_DQ_11)
HPS_DDR, (, , , , HPS_DQ_12, HPS_DQ_12)
HPS_DDR, (, , , , HPS_DQ_13, HPS_DQ_13)
HPS_DDR, (, , , , HPS_DQ_14, HPS_DQ_14)
HPS_DDR, (, , , , HPS_DQ_15, HPS_DQ_15)

HPS_DDR, (, , , , HPS_DQS_0, HPS_DQS_0)
HPS_DDR, (, , , , HPS_DQS#_0, HPS_DQS#_0)
HPS_DDR, (, , , , HPS_DQS_1, HPS_DQS_1)
HPS_DDR, (, , , , HPS_DQS#_1, HPS_DQS#_1)

HPS_DDR, (, , , , HPS_DM_0, HPS_DM_0)
HPS_DDR, (, , , , HPS_DM_1, HPS_DM_1)

HPS_DDR, (, , , , HPS_ODT_0, HPS_ODT_0)
HPS_DDR, (, , , , HPS_ODT_1, HPS_ODT_1)

HPS_RZQ_0

5CSXFC6G6U23I7N

C28 HPS_DDR3_ADDR0 << HPS_DDR3_ADDR0
B28 HPS_DDR3_ADDR1 << HPS_DDR3_ADDR1
E26 HPS_DDR3_ADDR2 << HPS_DDR3_ADDR2
D26 HPS_DDR3_ADDR3 << HPS_DDR3_ADDR3
J21 HPS_DDR3_ADDR4 << HPS_DDR3_ADDR4
J20 HPS_DDR3_ADDR5 << HPS_DDR3_ADDR5
C26 HPS_DDR3_ADDR6 << HPS_DDR3_ADDR6
B26 HPS_DDR3_ADDR7 << HPS_DDR3_ADDR7
E26 HPS_DDR3_ADDR8 << HPS_DDR3_ADDR8
F25 HPS_DDR3_ADDR9 << HPS_DDR3_ADDR9
A24 HPS_DDR3_ADDR10 << HPS_DDR3_ADDR10
B24 HPS_DDR3_ADDR11 << HPS_DDR3_ADDR11
D24 HPS_DDR3_ADDR12 << HPS_DDR3_ADDR12
C24 HPS_DDR3_ADDR13 << HPS_DDR3_ADDR13
G23 HPS_DDR3_ADDR14 << HPS_DDR3_ADDR14
F24 HPS_DDR3_ADDR15 << HPS_DDR3_ADDR15

A27 HPS_DDR3_BA0 << HPS_DDR3_BA0
H25 HPS_DDR3_BA1 << HPS_DDR3_BA1
G25 HPS_DDR3_BA2 << HPS_DDR3_BA2

N21 HPS_DDR3_CK_P << HPS_DDR3_CK_P
N20 HPS_DDR3_CK_N << HPS_DDR3_CK_N
L28 HPS_DDR3_CKE0 << HPS_DDR3_CKE0

E25 HPS_DDR3_WE_N << HPS_DDR3_WE_N
A26 HPS_DDR3_CAS_N << HPS_DDR3_CAS_N
A25 HPS_DDR3_RAS_N << HPS_DDR3_RAS_N
L21 HPS_DDR3_CS0_N << HPS_DDR3_CS0_N

J25 HPS_DDR3_DQ0 << HPS_DDR3_DQ0
J24 HPS_DDR3_DQ1 << HPS_DDR3_DQ1
E28 HPS_DDR3_DQ2 << HPS_DDR3_DQ2
D27 HPS_DDR3_DQ3 << HPS_DDR3_DQ3
J26 HPS_DDR3_DQ4 << HPS_DDR3_DQ4
K26 HPS_DDR3_DQ5 << HPS_DDR3_DQ5
G27 HPS_DDR3_DQ6 << HPS_DDR3_DQ6
F28 HPS_DDR3_DQ7 << HPS_DDR3_DQ7
K25 HPS_DDR3_DQ8 << HPS_DDR3_DQ8
L25 HPS_DDR3_DQ9 << HPS_DDR3_DQ9
J27 HPS_DDR3_DQ10 << HPS_DDR3_DQ10
J28 HPS_DDR3_DQ11 << HPS_DDR3_DQ11
M27 HPS_DDR3_DQ12 << HPS_DDR3_DQ12
M26 HPS_DDR3_DQ13 << HPS_DDR3_DQ13
M28 HPS_DDR3_DQ14 << HPS_DDR3_DQ14
N28 HPS_DDR3_DQ15 << HPS_DDR3_DQ15

R17 HPS_DDR3_DQS_P0 << HPS_DDR3_DQS_P0
R16 HPS_DDR3_DQS_N0 << HPS_DDR3_DQS_N0
R19 HPS_DDR3_DQS_P1 << HPS_DDR3_DQS_P1
R18 HPS_DDR3_DQS_N1 << HPS_DDR3_DQS_N1

G28 HPS_DDR3_DM0 << HPS_DDR3_DM0
P28 HPS_DDR3_DM1 << HPS_DDR3_DM1

D28 HPS_DDR3_ODT0 << HPS_DDR3_ODT0

D25 HPS_DDR3_RZQ R62 100R
GND

U3G

BANK 6B

HPS_DDR, (, , , , HPS_DQ_16, HPS_DQ_16)
HPS_DDR, (, , , , HPS_DQ_17, HPS_DQ_17)
HPS_DDR, (, , , , HPS_DQ_18, HPS_DQ_18)
HPS_DDR, (, , , , HPS_DQ_19, HPS_DQ_19)
HPS_DDR, (, , , , HPS_DQ_20, HPS_DQ_20)
HPS_DDR, (, , , , HPS_DQ_21, HPS_DQ_21)
HPS_DDR, (, , , , HPS_DQ_22, HPS_DQ_22)
HPS_DDR, (, , , , HPS_DQ_23, HPS_DQ_23)
HPS_DDR, (, , , , HPS_DQ_24, HPS_DQ_24)
HPS_DDR, (, , , , HPS_DQ_25, HPS_DQ_25)
HPS_DDR, (, , , , HPS_DQ_26, HPS_DQ_26)
HPS_DDR, (, , , , HPS_DQ_27, HPS_DQ_27)
HPS_DDR, (, , , , HPS_DQ_28, HPS_DQ_28)
HPS_DDR, (, , , , HPS_DQ_29, HPS_DQ_29)
HPS_DDR, (, , , , HPS_DQ_30, HPS_DQ_30)
HPS_DDR, (, , , , HPS_DQ_31, HPS_DQ_31)
HPS_DDR, (, , , , HPS_DQ_32, HPS_DQ_32)
HPS_DDR, (, , , , HPS_DQ_33, HPS_DQ_33)
HPS_DDR, (, , , , HPS_DQ_34, HPS_DQ_34)
HPS_DDR, (, , , , HPS_DQ_35, HPS_DQ_35)
HPS_DDR, (, , , , HPS_DQ_36, HPS_DQ_36)
HPS_DDR, (, , , , HPS_DQ_37, HPS_DQ_37)
HPS_DDR, (, , , , HPS_DQ_38, HPS_DQ_38)
HPS_DDR, (, , , , HPS_DQ_39, HPS_DQ_39)

HPS_DDR, (, , , , HPS_DQS_2, HPS_DQS_2)
HPS_DDR, (, , , , HPS_DQS#_2, HPS_DQS#_2)
HPS_DDR, (, , , , HPS_DQS_3, HPS_DQS_3)
HPS_DDR, (, , , , HPS_DQS#_3, HPS_DQS#_3)
HPS_DDR, (, , , , HPS_DQS_4, HPS_DQS_4)
HPS_DDR, (, , , , HPS_DQS#_4, HPS_DQS#_4)

HPS_DDR, (, , , , HPS_DM_2, HPS_DM_2)
HPS_DDR, (, , , , HPS_DM_3, HPS_DM_3)
HPS_DDR, (, , , , HPS_DM_4, HPS_DM_4)

HPS_DDR, (, , , , HPS_RESET#, HPS_RESET#)

N24 HPS_DDR3_DQ16 << HPS_DDR3_DQ16
N25 HPS_DDR3_DQ17 << HPS_DDR3_DQ17
J28 HPS_DDR3_DQ18 << HPS_DDR3_DQ18
J28 HPS_DDR3_DQ19 << HPS_DDR3_DQ19
N26 HPS_DDR3_DQ20 << HPS_DDR3_DQ20
N27 HPS_DDR3_DQ21 << HPS_DDR3_DQ21
R27 HPS_DDR3_DQ22 << HPS_DDR3_DQ22
V27 HPS_DDR3_DQ23 << HPS_DDR3_DQ23
R26 HPS_DDR3_DQ24 << HPS_DDR3_DQ24
R25 HPS_DDR3_DQ25 << HPS_DDR3_DQ25
AA28 HPS_DDR3_DQ26 << HPS_DDR3_DQ26
W26 HPS_DDR3_DQ27 << HPS_DDR3_DQ27
R24 HPS_DDR3_DQ28 << HPS_DDR3_DQ28
T24 HPS_DDR3_DQ29 << HPS_DDR3_DQ29
V27 HPS_DDR3_DQ30 << HPS_DDR3_DQ30
AA27 HPS_DDR3_DQ31 << HPS_DDR3_DQ31

T26
J25
AC28
V25
V19
V20
AE27
AD28

T19 HPS_DDR3_DQS_P2 << HPS_DDR3_DQS_P2
T18 HPS_DDR3_DQS_N2 << HPS_DDR3_DQS_N2
U19 HPS_DDR3_DQS_P3 << HPS_DDR3_DQS_P3
T20 HPS_DDR3_DQS_N3 << HPS_DDR3_DQS_N3

V18
V17

W28 HPS_DDR3_DM2 << HPS_DDR3_DM2
AB28 HPS_DDR3_DM3 << HPS_DDR3_DM3
AE28

V28 HPS_DDR3_RESET_N << HPS_DDR3_RESET_N

5CSXFC6G6U23I7N

HPS_DDR3_ADDR[14..0] << HPS_DDR3_ADDR[14..0]

HPS_DDR3_DQ[31..0] << HPS_DDR3_DQ[31..0]

HPS_DDR3_BA[2..0] << HPS_DDR3_BA[2..0]

HPS_DDR3_DM[3..0] << HPS_DDR3_DM[3..0]

HPS_DDR3_DQS_P[3..0] << HPS_DDR3_DQS_P[3..0]

HPS_DDR3_DQS_N[3..0] << HPS_DDR3_DQS_N[3..0]

HPS_DDR3_ADDR15 << HPS_DDR3_ADDR15

HPS_DDR3_CK_P << HPS_DDR3_CK_P

HPS_DDR3_CK_N << HPS_DDR3_CK_N

HPS_DDR3_CKE0 << HPS_DDR3_CKE0

HPS_DDR3_CS0_N << HPS_DDR3_CS0_N

HPS_DDR3_RESET_N << HPS_DDR3_RESET_N

HPS_DDR3_WE_N << HPS_DDR3_WE_N

HPS_DDR3_RAS_N << HPS_DDR3_RAS_N

HPS_DDR3_CAS_N << HPS_DDR3_CAS_N

HPS_DDR3_ODT0 << HPS_DDR3_ODT0

Title		
Size	Number	Revision
A4		
Date:	2-18-2025	Sheet of
File:	E:\小梅哥\FPGA同步空间\HPS_6A6B\DDR3_6B\DDR3_6B.schDoc	

U3K

BANK 7D

RGMII0_TX_CLK, (, , , , , , RGMII0_TX_CLK, , , HPS_GPIO0)
RGMII0_TXD0, (, , , , , , RGMII0_TXD0, USB1_D0, , HPS_GPIO1)
RGMII0_TXD1, (, , , , , , RGMII0_TXD1, USB1_D1, , HPS_GPIO2)
RGMII0_TXD2, (, , , , , , RGMII0_TXD2, USB1_D2, , HPS_GPIO3)
RGMII0_TXD3, (, , , , , , RGMII0_TXD3, USB1_D3, , HPS_GPIO4)
RGMII0_RXD0, (, , , , , , RGMII0_RXD0, USB1_D4, , HPS_GPIO5)
RGMII0_MDIO, (, , , , , , RGMII0_MDIO, USB1_D5, I2C2_SDA, HPS_GPIO6)
RGMII0_MDC, (, , , , , , RGMII0_MDC, USB1_D6, I2C2_SCL, HPS_GPIO7)
RGMII0_RX_CTL, (, , , , , , RGMII0_RX_CTL, USB1_D7, , HPS_GPIO8)
RGMII0_TX_CTL, (, , , , , , RGMII0_TX_CTL, , , HPS_GPIO9)
RGMII0_RX_CLK, (, , , , , , RGMII0_RX_CLK, USB1_CLK, , HPS_GPIO10)
RGMII0_RXD1, (, , , , , , RGMII0_RXD1, USB1_STP, , HPS_GPIO11)
RGMII0_RXD2, (, , , , , , RGMII0_RXD2, USB1_DIR, , HPS_GPIO12)
RGMII0_RXD3, (, , , , , , RGMII0_RXD3, USB1_NXT, , HPS_GPIO13)

E4 HPS_GPIO0
C10 HPS_GPIO1 USB_DATA0
F5 HPS_GPIO2 USB_DATA1
C9 HPS_GPIO3 USB_DATA2
C4 HPS_GPIO4 USB_DATA3
C8 HPS_GPIO5 USB_DATA4
D4 HPS_GPIO6 USB_DATA5
C7 HPS_GPIO7 USB_DATA6
F4 HPS_GPIO8 USB_DATA7
C6 HPS_GPIO9
G4 HPS_GPIO10 USB_CLKOUT
E5 HPS_GPIO11 USB_STP
E5 HPS_GPIO12 USB_DIR
D5 HPS_GPIO13 USB_NXT

HPS_GPIO0
HPS_GPIO1_USB_DATA0
HPS_GPIO2_USB_DATA1
HPS_GPIO2_USB_DATA2
HPS_GPIO2_USB_DATA3
HPS_GPIO2_USB_DATA4
HPS_GPIO2_USB_DATA5
HPS_GPIO2_USB_DATA6
HPS_GPIO2_USB_DATA7
HPS_GPIO9
HPS_GPIO10_USB_CLKOUT
HPS_GPIO11_USB_STP
HPS_GPIO11_USB_STP
HPS_GPIO12_USB_DIR
HPS_GPIO13_USB_NXT

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U3I

BANK 7B

NAND_ALE, (, , , , , , NAND_ALE, RGMII1_TX_CLK, QSPL_SS3, HPS_GPIO14)
NAND_CE, (, , , , , , NAND_CE, RGMII1_TXD0, USB1_D0, HPS_GPIO15)
NAND_CLE, (, , , , , , NAND_CLE, RGMII1_TXD1, USB1_D1, HPS_GPIO16)
NAND_RE, (, , , , , , NAND_RE, RGMII1_TXD2, USB1_D2, HPS_GPIO17)
NAND_RB, (, , , , , , NAND_RB, RGMII1_TXD3, USB1_D3, HPS_GPIO18)
NAND_DQ0, (, , , , , , NAND_DQ0, RGMII1_RXD0, , HPS_GPIO19)
NAND_DQ1, (, , , , , , NAND_DQ1, RGMII1_MDIO, I2C3_SDA, HPS_GPIO20)
NAND_DQ2, (, , , , , , NAND_DQ2, RGMII1_MDC, I2C3_SCL, HPS_GPIO21)
NAND_DQ3, (, , , , , , NAND_DQ3, RGMII1_RX_CTL, USB1_D4, HPS_GPIO22)
NAND_DQ4, (, , , , , , NAND_DQ4, RGMII1_TX_CTL, USB1_D5, HPS_GPIO23)
NAND_DQ5, (, , , , , , NAND_DQ5, RGMII1_RX_CLK, USB1_D6, HPS_GPIO24)
NAND_DQ6, (, , , , , , NAND_DQ6, RGMII1_RXD1, USB1_D7, HPS_GPIO25)
NAND_DQ7, (, , , , , , NAND_DQ7, RGMII1_RXD2, , HPS_GPIO26)
NAND_WP, (, , , , , , NAND_WP, RGMII1_RXD3, QSPL_SS2, HPS_GPIO27)
NAND_WE, BOOTSEL2, (, , , , , , NAND_WE, QSPL_SS1, , HPS_GPIO28)
QSPL_IO0, (, , , , , , QSPL_IO0, , USB1_CLK, HPS_GPIO29)
QSPL_IO1, (, , , , , , QSPL_IO1, , USB1_STP, HPS_GPIO30)
QSPL_IO2, (, , , , , , QSPL_IO2, , USB1_DIR, HPS_GPIO31)
QSPL_IO3, (, , , , , , QSPL_IO3, , USB1_NXT, HPS_GPIO32)
QSPL_SS0, BOOTSEL1, (, , , , , , QSPL_SS0, , , HPS_GPIO33)
QSPL_CLK, (, , , , , , QSPL_CLK, , , HPS_GPIO34)
QSPL_SS1, (, , , , , , QSPL_SS1, , , HPS_GPIO35)

J15 HPS_GPIO14 ENET1 GTX_CLK
A16 HPS_GPIO15 ENET1_TX_DATA0
J14 HPS_GPIO16 ENET1_TX_DATA1
A15 HPS_GPIO17 ENET1_TX_DATA2
D17 HPS_GPIO18 ENET1_TX_DATA3
A14 HPS_GPIO19 ENET1_RX_DATA0
E16 HPS_GPIO20 ENET1_MDIO
A13 HPS_GPIO21 ENET1_MDC
J13 HPS_GPIO22 ENET1_RX_DV
A12 HPS_GPIO23 ENET1_TX_EN
J12 HPS_GPIO24 ENET1_RX_CLK
A11 HPS_GPIO25 ENET1_RX_DATA1
C15 HPS_GPIO26 ENET1_RX_DATA2
A9 HPS_GPIO27 ENET1_RX_DATA3
D15 HPS_BOOTSEL2
A8 QSPL_DATA0
H16 QSPL_DATA1
A7 QSPL_DATA2
J16 QSPL_DATA3
A6 HPS_BOOTSEL1 QSPL_SS
C14 QSPL_DCLK
B14 HPS_GPIO35

HPS_GPIO14_ENET1_GTX_CLK
HPS_GPIO15_ENET1_TX_DATA0
HPS_GPIO16_ENET1_TX_DATA1
HPS_GPIO17_ENET1_TX_DATA2
HPS_GPIO18_ENET1_TX_DATA3
HPS_GPIO19_ENET1_RX_DATA0
HPS_GPIO20_ENET1_MDIO
HPS_GPIO21_ENET1_MDC
HPS_GPIO22_ENET1_RX_DV
HPS_GPIO23_ENET1_TX_EN
HPS_GPIO24_ENET1_RX_CLK
HPS_GPIO25_ENET1_RX_DATA1
HPS_GPIO26_ENET1_RX_DATA2
HPS_GPIO27_ENET1_RX_DATA3
HPS_BOOTSEL2
QSPL_DATA0
QSPL_DATA1
QSPL_DATA2
QSPL_DATA3
QSPL_SS
QSPL_DCLK
HPS_GPIO35

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U3H

BANK 7A

TRACE_CLK, (, , , , , , TRACE_CLK, , , HPS_GPIO48)
TRACE_D0, (, , , , , , TRACE_D0, SPIS0_CLK, UART0_RX, HPS_GPIO49)
TRACE_D1, (, , , , , , TRACE_D1, SPIS0_MOSI, UART0_TX, HPS_GPIO50)
TRACE_D2, (, , , , , , TRACE_D2, SPIS0_MISO, I2C1_SDA, HPS_GPIO51)
TRACE_D3, (, , , , , , TRACE_D3, SPIS0_SS0, I2C1_SCL, HPS_GPIO52)
TRACE_D4, (, , , , , , TRACE_D4, SPIS1_CLK, CAN1_RX, HPS_GPIO53)
TRACE_D5, (, , , , , , TRACE_D5, SPIS1_MOSI, CAN1_TX, HPS_GPIO54)
TRACE_D6, (, , , , , , TRACE_D6, SPIS1_SS0, I2C0_SDA, HPS_GPIO55)
TRACE_D7, (, , , , , , TRACE_D7, SPIS1_MISO, I2C0_SCL, HPS_GPIO56)
SPIM0_CLK, (, , , , , , SPIM0_CLK, I2C1_SDA, UART0_CTS, HPS_GPIO57)
SPIM0_MOSI, (, , , , , , SPIM0_MOSI, I2C1_SCL, UART0_RTS, HPS_GPIO58)
SPIM0_MISO, (, , , , , , SPIM0_MISO, CAN1_RX, UART1_CTS, HPS_GPIO59)
SPIM0_SS0, BOOTSEL0, (, , , , , , SPIM0_SS0, CAN1_TX, UART1_RTS, HPS_GPIO60)
UART0_RX, (, , , , , , UART0_RX, CAN0_RX, SPIM0_SS1, HPS_GPIO61)
UART0_TX, CLKSEL1, (, , , , , , UART0_TX, CAN0_TX, SPIM1_SS1, HPS_GPIO62)
I2C0_SDA, (, , , , , , I2C0_SDA, UART1_RX, SPIM1_CLK, HPS_GPIO63)
I2C0_SCL, (, , , , , , I2C0_SCL, UART1_TX, SPIM1_MOSI, HPS_GPIO64)
CAN0_RX, (, , , , , , CAN0_RX, UART0_RX, SPIM1_MISO, HPS_GPIO65)
CAN0_TX, CLKSEL0, (, , , , , , CAN0_TX, UART0_TX, SPIM1_SS0, HPS_GPIO66)

C21 HPS_GPIO48
A22 HPS_GPIO49 UART_RXD
B21 HPS_GPIO50 UART_TXD
A21 HPS_GPIO51
K18 HPS_GPIO52
A20 HPS_GPIO53
J18 HPS_GPIO54
A19 HPS_GPIO55 I2C_SDA
C18 HPS_GPIO56 I2C_SCL
A18 HPS_GPIO57
C17 HPS_GPIO58
B18 HPS_GPIO59
J17 HPS_BOOTSEL0 HPS_SPIM0_SS
A17 HPS_GPIO61
H17 HPS_CLOCKSEL1 HPS_GPIO62
C19 HPS_SPIM1_CLK HPS_GPIO63
B16 HPS_SPIM1_MOSI HPS_GPIO64
B19 HPS_SPIM1_MISO HPS_GPIO65
C16 HPS_SPIM1_SS HPS_GPIO66

HPS_GPIO48
HPS_GPIO49_UART_RXD
HPS_GPIO50_UART_TXD
HPS_GPIO51
HPS_GPIO52
HPS_GPIO53
HPS_GPIO54
HPS_GPIO55_I2C_SDA
HPS_GPIO56_I2C_SCL
HPS_GPIO57
HPS_GPIO58
HPS_GPIO59
HPS_GPIO61
HPS_GPIO62
HPS_GPIO63
HPS_GPIO64
HPS_GPIO65
HPS_GPIO66

VCCIO7
R63
10K

Title		
Size	Number	Revision
A4		
Date:	2-18-2025	Sheet of
File:	E:\小梅哥\FPGA同步空间\HPS_7A7BDD\GPIO_SchDoc	

